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# Jinmao

CPU : Arrandale PGA

Chip Set : Intel Ibex Peak

GFX : N12M / INT.GFX

Remarks : Calpella Platform

Model Name : Jinmao

PBA Name : MAIN

PCB Code : BA41-01432A (GCE)  
BA41-01433A (NY)  
BA41-01434A (HAN)  
BA41-01435A (GBM)

Dev. Step : PR

Revision : 1.0

T.R. Date : 2010.11.26

Design	CHECK	APPROVAL
MS YANG	MK KIM	BL LEE

■ Owner : SEC IT Solution N/P LAB Signature : mansu

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DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR	MAIN		ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0	COVER	PART NO.	BA41-01432A
MODULE CODE		LAST EDIT	November 22, 2010 15:53:34 PM	PAGE	1	OF 52



BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails		Active in
VDC P12.0V_ALW P3.3V_MICOM P5.0V_ALW P5.0V_STB	Primary DC system power supply (7 to 21V) 12.0V always power rail 3.3V always power rail (for Micom) 5.0V always power rail 5.0V always power rail	S4 - S5
P5.0V_AUX P3.3V_AUX P1.5V_AUX	5.0V switched on power rail (off in S4-S5) 3.3V switched on power rail (off in S4-S5) 1.5V power rail for DDR (off in S4-S5)	S3
P5.0V P3.3V P1.8V P1.5V P1.05V P0.75V	5.0V switched power rail (off in S3-S5) 3.3V switched power rail (off in S3-S5) 1.8V switched power rail (off in S3-S5) 1.5V switched power rail (off in S3-S5) 1.05V power rail for chipset (off in S3-S5) 0.9V power rail for DDR (off in S3-S5)	S0
VCC_CORE IGFX_CORE EGFX_CORE P1.05V (VCCP)	Core Voltage for CPU Core Voltage for IGFX Core Voltage for GPU VCC for Arrandale & IBEX Peak	S0

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	1	Mini Card 1 (WLAN)
1	SYSTEM PORT 1	2	NC
2	Mini PCI Express	3	NC
3	Multi Memory Card Controller	4	LAN CONTROLLER
4	NC	5	NC
5	NC	6	NC
6	NC (N/A WITH HM55)	7	NC (N/A WITH HM55)
7	NC (N/A WITH HM55)	8	NC (N/A WITH HM55)
8	NC		
9	SYSTEM PORT 2 (SUB BOARD)		
10	Bluetooth		
11	Camera		
12	NC		
13	NC		

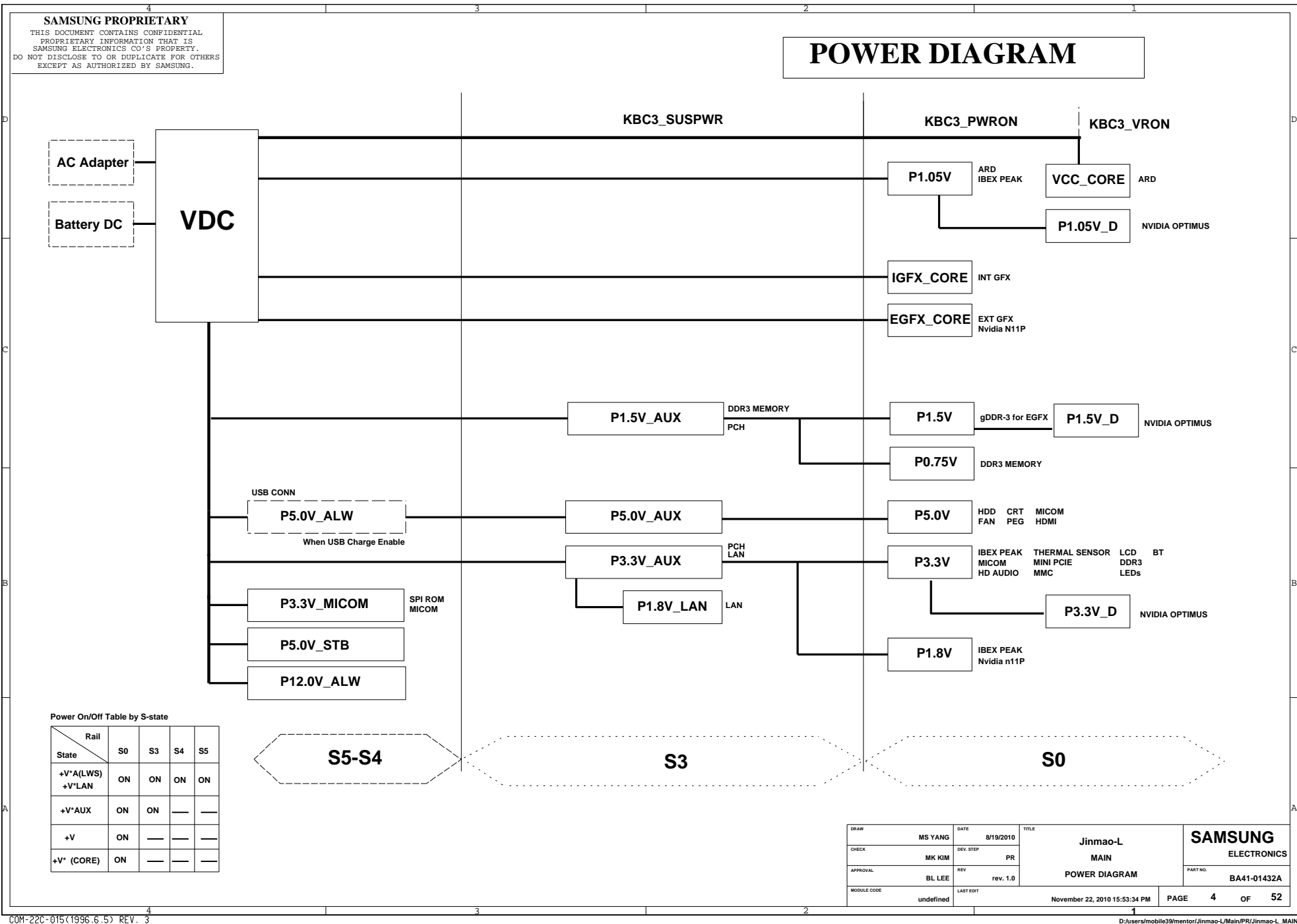
SATA PORT Assign	
PORT #	ASSIGNED TO
0	HDD
1	ODD
2	(N/A WITH HM55)
3	(N/A WITH HM55)
4	
5	

Crystal / Oscillator			
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	IBEX-PEAK	Real Time Clock
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN

LCD Pannel Detect		
Devices	Resolution	PANNEL_DETECT_0
LTN140AT17	HD(1366x768)	SEC3250

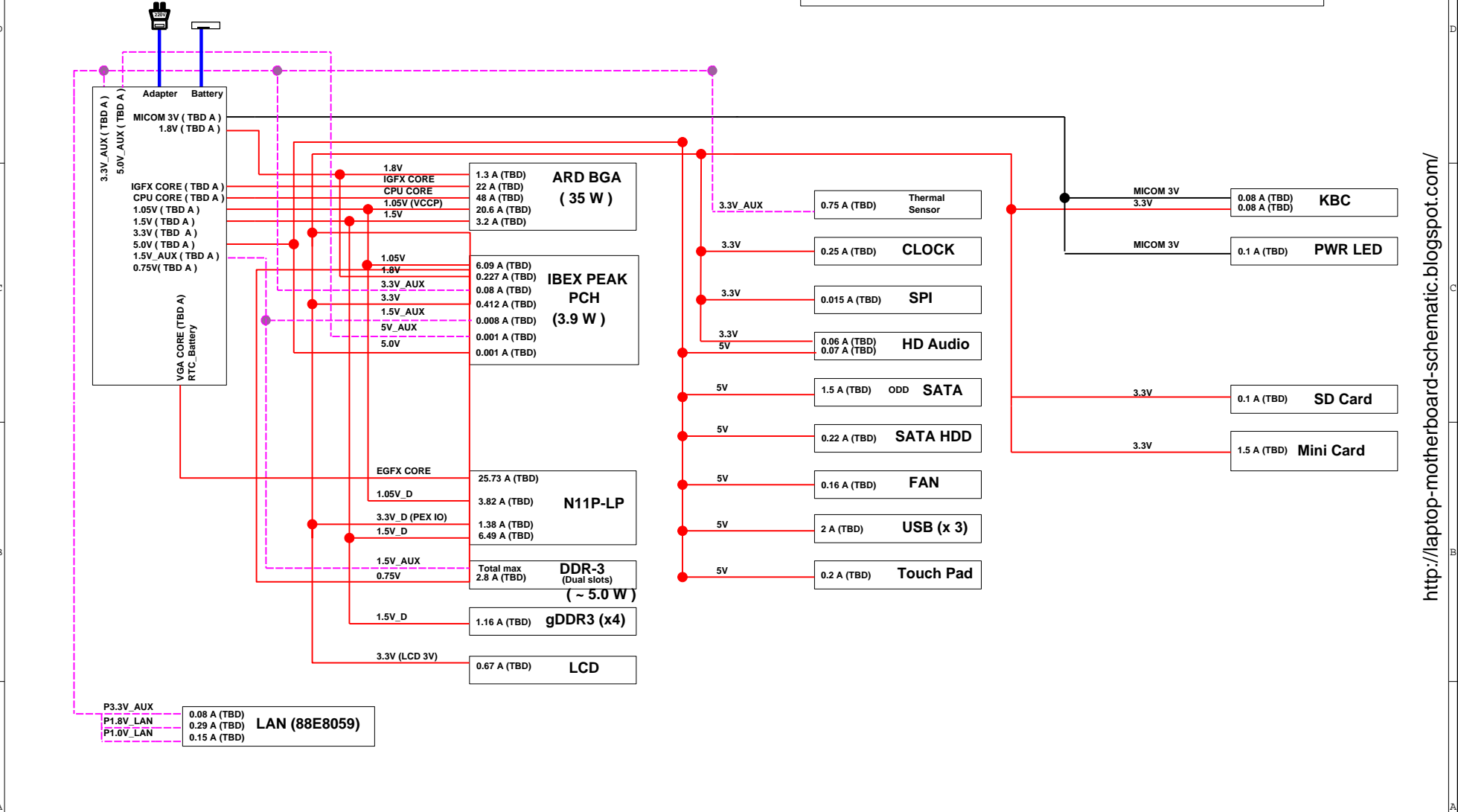
I <sup>2</sup> C / SMB Address			
Devices	Address	Hex	Bus
IBEX PEAK	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	
SODIMM0	1010 000x	A0h	Thermal Sensor
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M Shrink(Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
Thermal Sensor on board	1101 100x	98h	
Power thermal management TS	1101 011x	96h	

DRAW	MS YANG	DATE	8/19/2010	Jinmao-L MAIN BOARD INFO	SAMSUNG ELECTRONICS PART NO. BA41-01432A
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# POWER RAILS ANALYSIS



<http://laptop-motherboard-schematic.blogspot.com/>

DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L MAIN POWER RAILS	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR			PART NO. BA41-01432A
APPROVAL	BL LEE	REV	rev. 1.0			
MODULE CODE	undefined	LAST EDIT	November 22, 2010 15:53:34 PM	PAGE	5	OF 52

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# POWER SEQUENCE

Rev. 1.0

The diagram illustrates the power sequence for a system. It shows the interconnections between various components and their power management ICs. The components include:

- KBC (MEC1300-NU)**: The main control unit, receiving VDC and ADT3\_SEL# signals. It controls the ISL6255 CHARGER, ISL62882 CPU\_CORE, and the PCH.
- PCH (Platform Controller Hub)**: Receives signals from the KBC and controls the ARD (Advanced RISC Die), SPI ROM, and various power management ICs.
- ARD (Advanced RISC Die)**: Receives signals from the PCH and controls the VTT\_PWRGD signal.
- ISL6255 CHARGER**: Receives VDC and ADT3\_SEL# signals.
- ISL62882 CPU\_CORE**: Receives signals from the KBC and controls the VRM3\_CLKPWRGD#\_INV and VRM3\_CPU\_PWRGD signals.
- TPS51125**: Receives KBC3\_SUSPWR and KBC3\_PWRON signals, providing P3.3V\_MICOM, P5.0V\_ALW, P5.0V\_AUX, and P3.3V\_AUX.
- RT8207 MEM POWER**: Receives KBC3\_PWRON and provides P1.5V\_AUX.
- SWITCHED POWER**: Receives KBC3\_PWRON and provides P1.5V, P3.3V, and P5.0V.
- APL5930 P1.8V**: Receives KBC3\_PWRON and provides P1.8V.
- RT8207 P0.75V**: Receives KBC3\_PWRON and provides P0.75V.
- TPS51117 CHIPSET POWER**: Receives KBC3\_PWRON and provides P1.05V.
- ISL958708 EGFX\_CORE**: Receives EGFX\_CORE\_PWREN and VRM3\_EGFX\_PWRGD signals, providing EGFX\_CORE.
- ADP3211 IGFX\_CORE**: Receives IGFX\_CORE\_PWREN and provides IGFX\_CORE.
- 88E8059 LAN MARVELL**: Receives P3.3V\_AUX and provides P1.8V\_LAN.

The diagram also shows the power management ICs and their outputs:

- ISL6255 CHARGER**: 2) VDC, 3-1) ADT3\_SEL#, 4) POWER\_SW#.
- ISL62882 CPU\_CORE**: 19-1) VRM3\_CLKPWRGD#\_INV, 19) VRM3\_CPU\_PWRGD, 18) KBC3\_VRON.
- TPS51125**: 3) P3.3V\_MICOM, 6) P5.0V\_ALW, 6) P5.0V\_AUX, 6) P3.3V\_AUX.
- RT8207 MEM POWER**: 6) P1.5V\_AUX.
- SWITCHED POWER**: 13) P1.5V, 13) P3.3V, 13) P5.0V.
- APL5930 P1.8V**: 13) P1.8V.
- RT8207 P0.75V**: 13) P0.75V.
- TPS51117 CHIPSET POWER**: 13) P1.05V.
- ISL958708 EGFX\_CORE**: 13) EGFX\_CORE, 14) VRM3\_EGFX\_PWRGD.
- ADP3211 IGFX\_CORE**: 16) IGFX\_CORE.
- 88E8059 LAN MARVELL**: 6-1) P1.8V\_LAN.

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- TPS51125**: 3) P3.3V\_MICOM, 6) P5.0V\_ALW, 6) P5.0V\_AUX, 6) P3.3V\_AUX.
- RT8207 MEM POWER**: 6) P1.5V\_AUX.
- SWITCHED POWER**: 13) P1.5V, 13) P3.3V, 13) P5.0V.
- APL5930 P1.8V**: 13) P1.8V.
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- RT8207 MEM POWER**: 6) P1.5V\_AUX.
- SWITCHED POWER**: 13) P1.5V, 13) P3.3V, 13) P5.0V.
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The diagram also shows the power management ICs and their outputs:

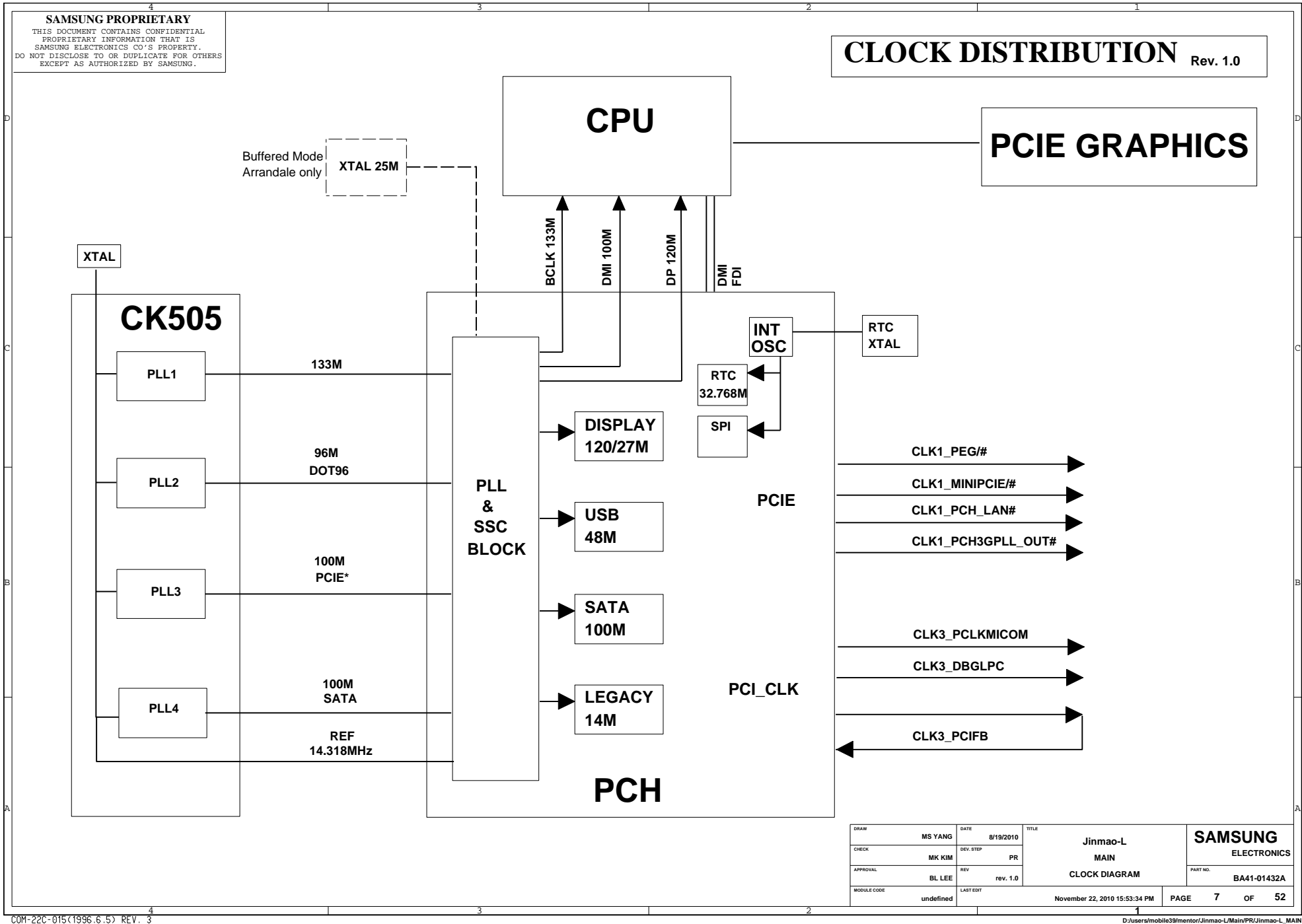
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- RT8207 MEM POWER**: 6) P1.5V\_AUX.
- SWITCHED POWER**: 13) P1.5V, 13) P3.3V, 13) P5.0V.
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- RT8207 MEM POWER**: 6) P1.5V\_AUX.
- SWITCHED POWER**: 13) P1.5V, 13) P3.3V, 13) P5.0V.
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- RT8207 MEM POWER**: 6) P1.5V\_AUX.
- SWITCHED POWER**: 13) P1.5V, 13) P3.3V, 13) P5.0V.
- APL5930 P1.8V**: 13) P1.8V.
- RT8207 P0.75V**:



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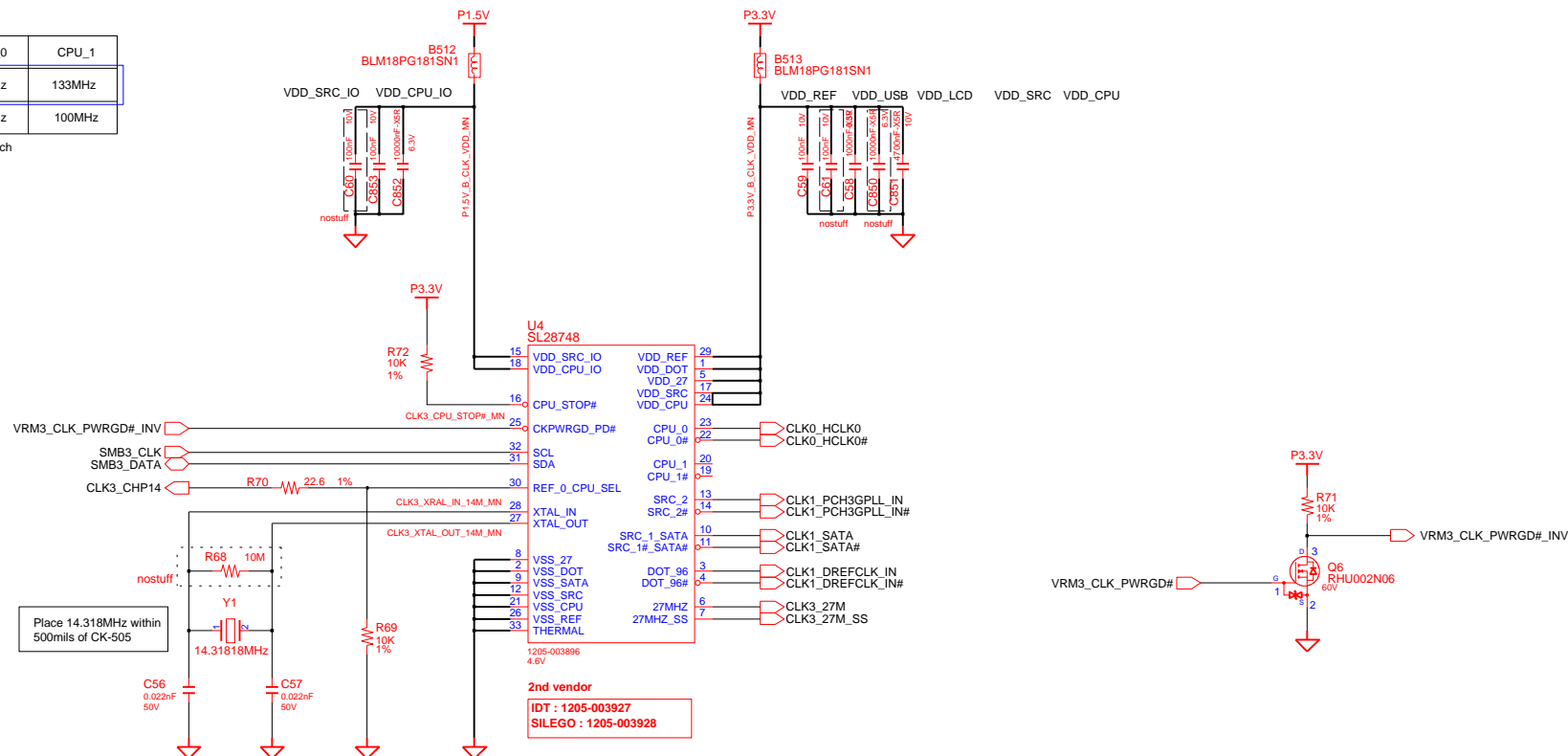
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## CK505M SHRINK VERSION

### CPU\_MODE SEL

Pin 30	CPU_0	CPU_1
CPU_SEL = 0	133MHz	133MHz
CPU_SEL = 1	100MHz	100MHz

\*CPU\_SEL During CK\_PWRGD Latch



DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L CLOCK CK505-SHRINK	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR			PART NO. BA41-01432A
APPROVAL	BL LEE	REV	rev. 1.0			
MODULE CODE		LAST EDIT		November 22, 2010 15:53:34 PM	PAGE 8 OF 52	



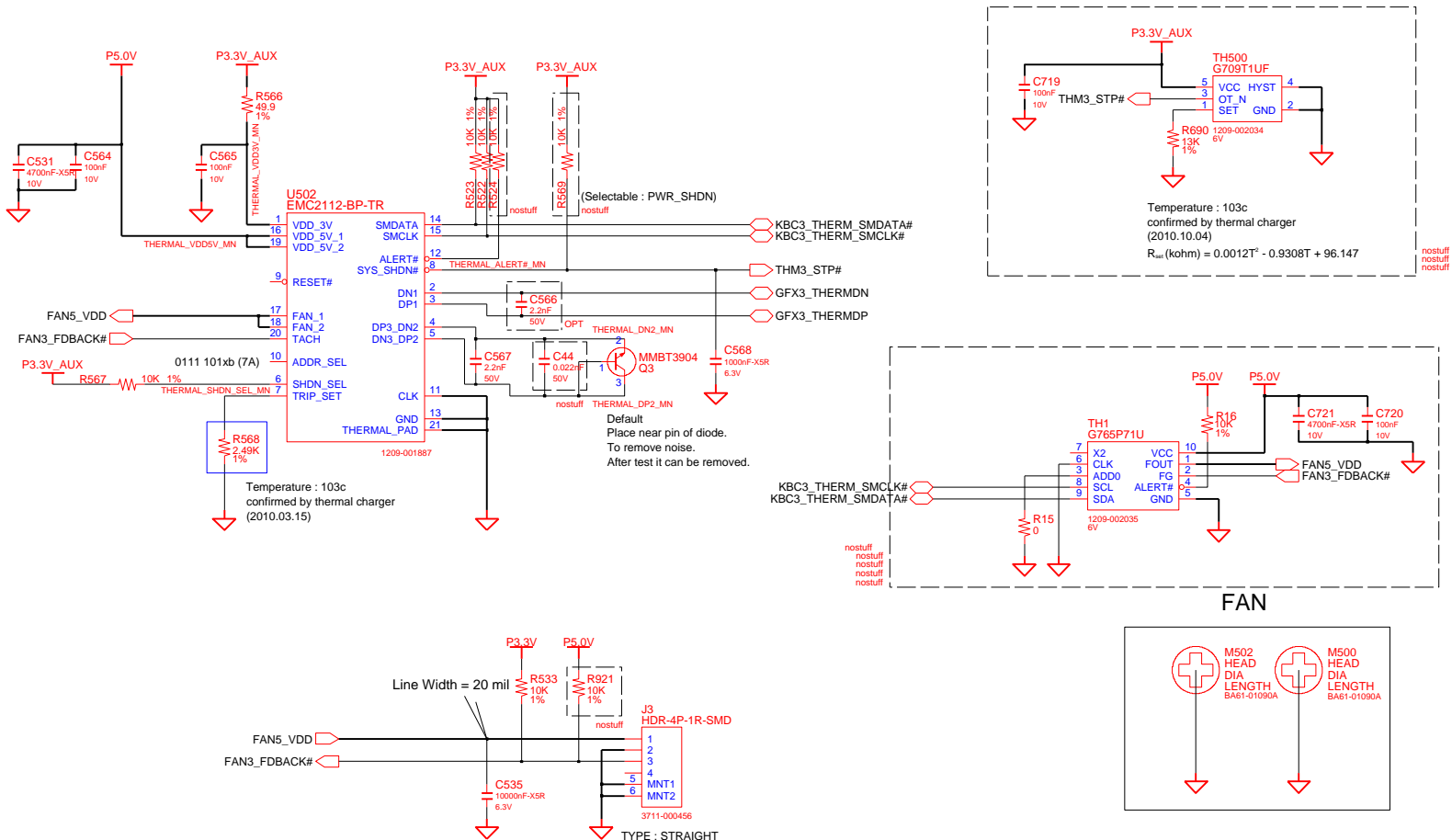
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# THERMAL SENSOR & FAN CONTROL

ADDRESSSEL MODE	
0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb

SHDNSEL MODE	
0	INTEL TR MODE
✓ HIGH Z	AMD CPU/DIODE MODE
1	EXT.DIODE 2 MODE

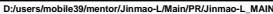


DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L
CHECK	MK KIM	DEV. STEP	PR		THERMAL SENSOR
APPROVAL	BL LEE	REV	rev. 1.0		THERMAL SENSOR EMC2112
MODULE CODE		LAST EDIT		November 22, 2010 15:53:34 PM	
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**SAMSUNG**  
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[illegible]



DRAW	MS YANG	DATE	8/19/2010	Jinmao-L CPU PGA CPU (2/4)		<b>SAMSUNG</b> ELECTRONICS	
CHECK	MK KIM	DEV. STEP	PR				
APPROVAL	BL LEE	REV	REV. 1.0				
				PART NO.		BA41-01432A	
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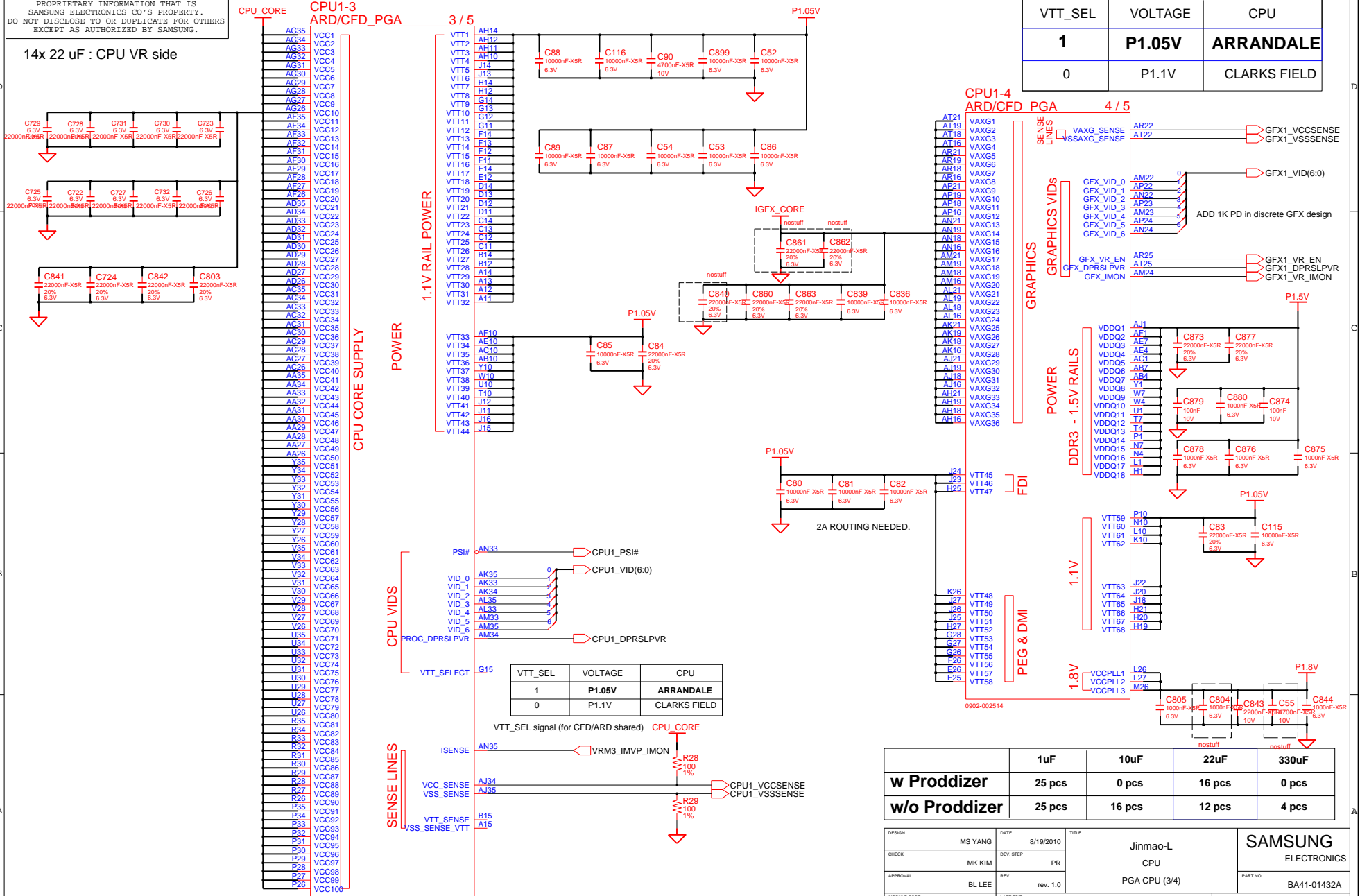
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14x 22 uF : CPU VR side

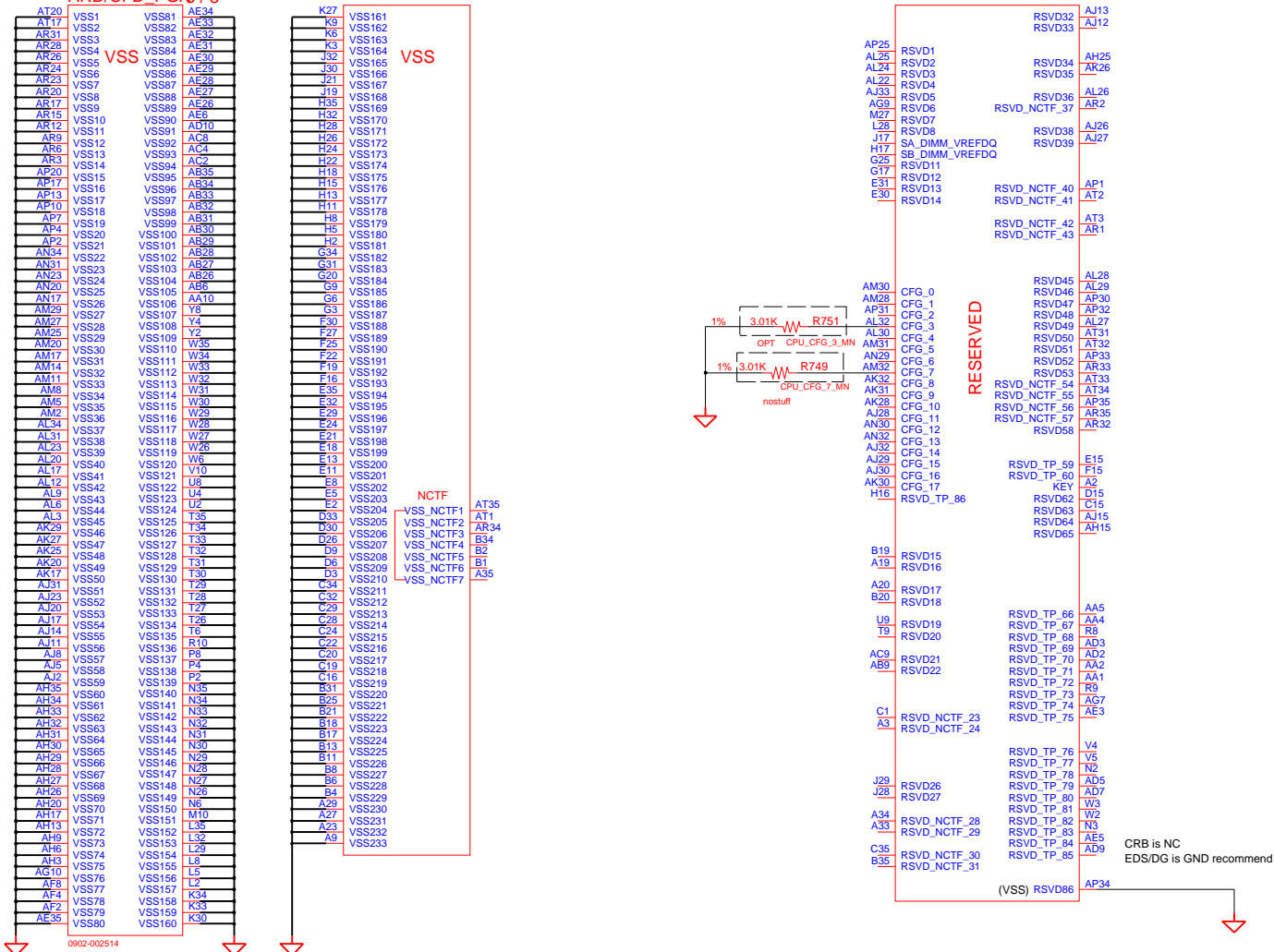
ALL VTT DECAP IS SHARED

\*\*VTT POWER SELECTION

VTT_SEL	VOLTAGE	CPU
1	P1.05V	ARRANDALE
0	P1.1V	CLARKS FIELD



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CPU1-5  
ARD/CFD\_PGA5 / 5

Clarksfield : SA\_DIMM\_VRREFDQ, 100K PD  
SB\_DIMM\_VRREFDQ, 100K PD

Arrandale : SA\_DIMM\_VRREFDQ, NC  
SB\_DIMM\_VRREFDQ, NC

### CFG Straps for Processor

PCI Express Configuration Select	
CFG0	1 : Single PEG 0 : Bifunction enabled
PCI Express Static Lane Reversal	
CFG3	1 : Normal operation 0 : Lane Reversed
Display Port Presence	
CFG4	1 : Disabled - No DP device is connected to eDP 0 : Enabled - (DP device is connected to eDP
PCIe 2.0 SUPPORT	
CFG7	1 : Normal operation 0 : PCIe2.0 Jitter support

DESIGN	MS YANG	DATE	8/19/2010	Jinmao-L CPU PGA CPU (4/4)	<b>SAMSUNG</b> ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR		
APPROVAL	BL LEE	REV	rev. 1.0		
MODULE CODE	LAST EDIT		November 22, 2010 15:53:34 PM PAGE 13 OF 52		

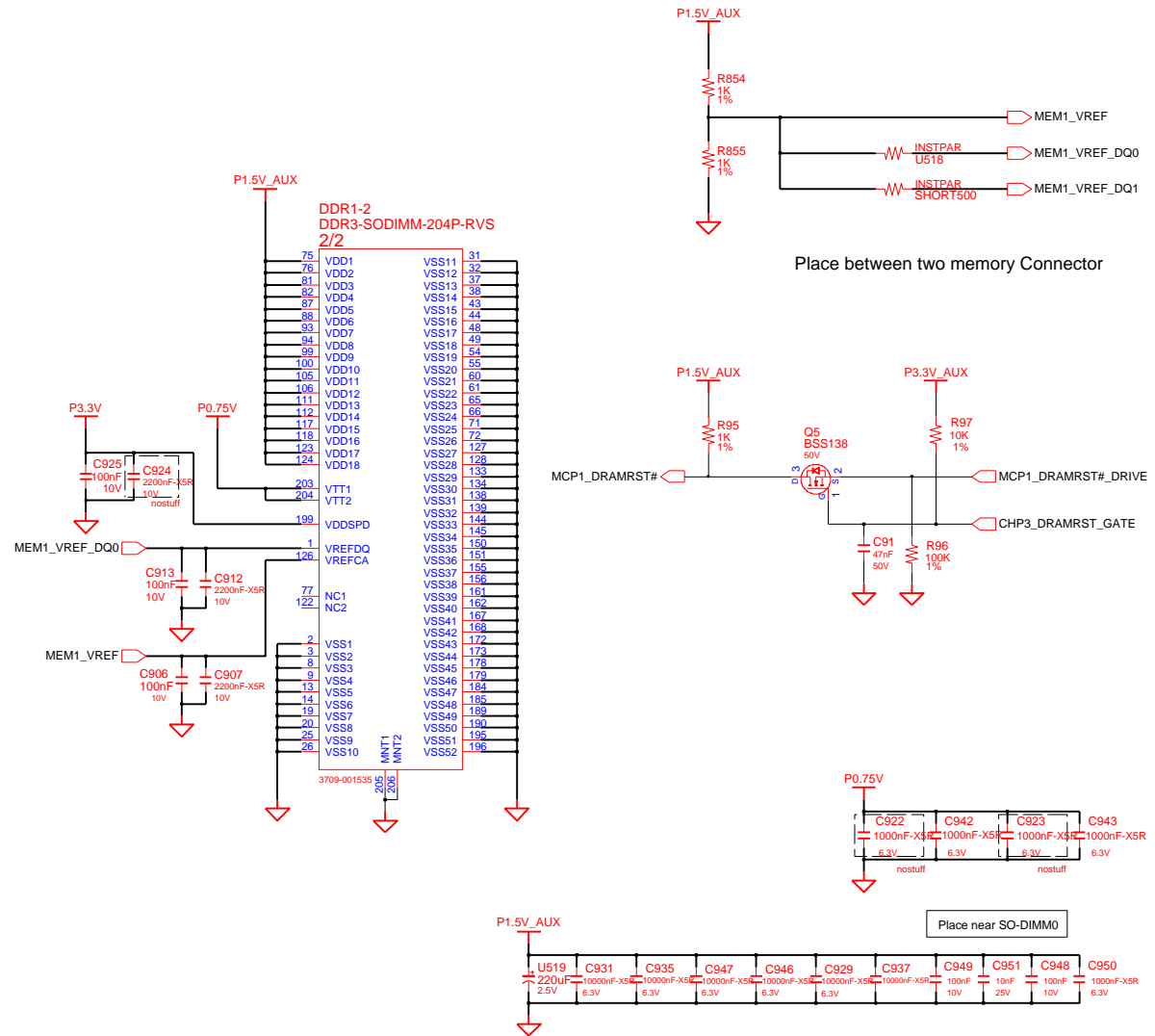
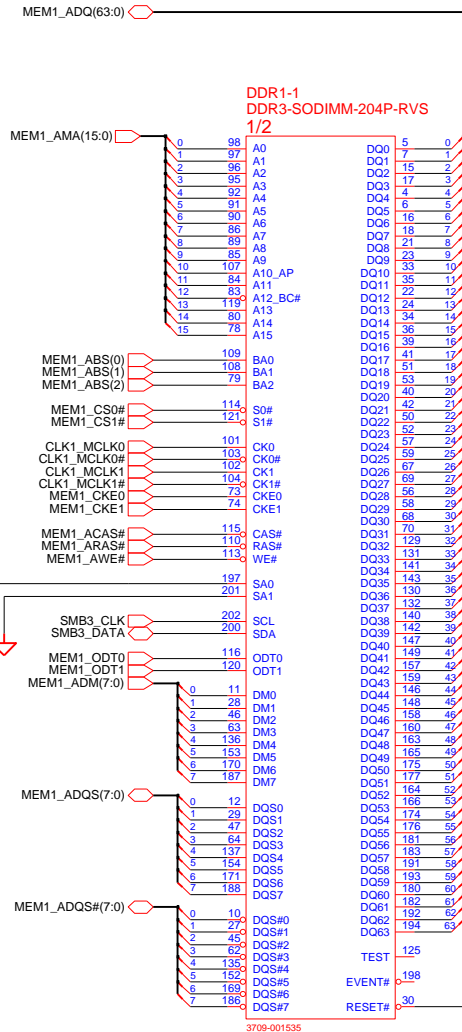
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## DDR SO-DIMM #0

Height : 9.2 mm (REVERSE)

P/N : 3709-001535 (FOXCONN)

P/N : 3709-001609 (CONCRAFT)



DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV STEP	PR		SODIMM A	
APPROVAL	BL LEE	REV	rev. 1.0		DDR3	
MODULE CODE		LAST EDIT				
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**DDR SO-DIMM #1**  
Height : 4 mm (REVERSE)

MEM1\_BDQ3(63:0)

MEM1\_BMA(15:0)

MEM1\_BBS(0)

MEM1\_BBS(1)

MEM1\_BBS(2)

MEM1\_CS2#

MEM1\_CS3#

CLK1\_MCLK2

CLK1\_MCLK2#

CLK1\_MCLK3

MEM1\_CKE2

MEM1\_CKE3

MEM1\_BCAS#

MEM1\_BRAS#

MEM1\_BWE#

SMB3\_CLK

SMB3\_DATA

MEM1\_ODT2

MEM1\_ODT3

MEM1\_BDM(7:0)

MEM1\_BDQS(7:0)

MEM1\_BDQS#(7:0)

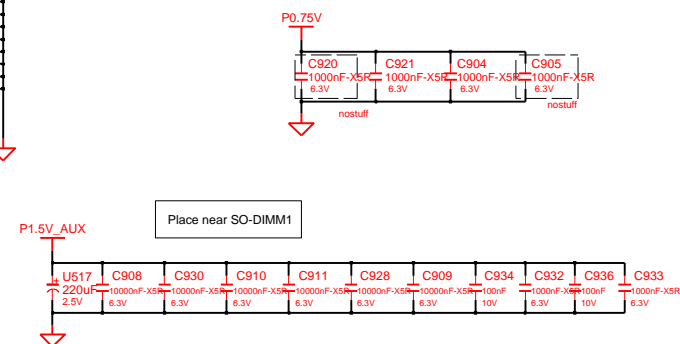
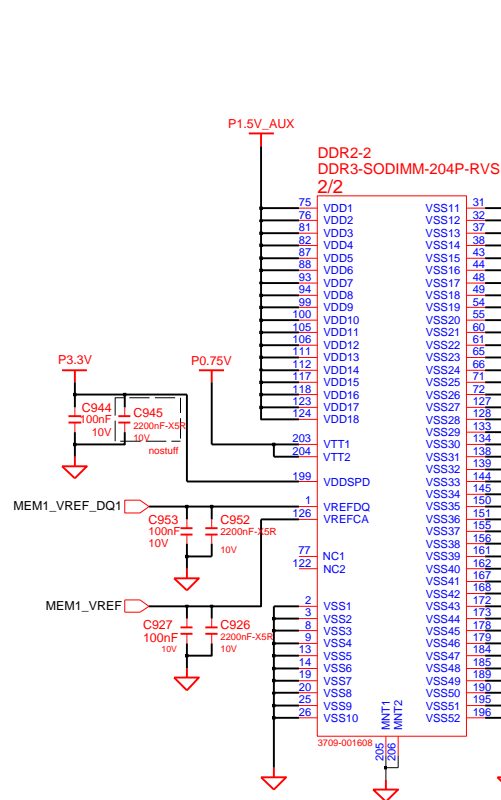
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 DDR3-SODIMM-204P-RVS  
 1/2

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1	97	A1	DQ1	7	1
2	96	A2	DQ2	15	2
3	95	A3	DQ3	17	3
4	92	A4	DQ4	4	4
5	91	A5	DQ5	6	5
6	90	A6	DQ6	16	6
7	86	A7	DQ7	18	7
8	89	A8	DQ8	21	8
9	85	A9	DQ9	23	9
10	107	A10	DQ10	33	10
11	84	A11	DQ11	35	11
12	83	A12	DQ12	22	12
13	119	A13	DQ13	24	13
14	80	A14	DQ14	34	14
15	78	A15	DQ15	36	15
			DQ16	38	16
			DQ17	41	17
			DQ18	51	18
			DQ19	53	19
			DQ20	42	21
			DQ21	50	22
			DQ22	52	23
			DQ23	52	23
			DQ24	59	24
			DQ25	67	26
			DQ26	67	26
			DQ27	69	27
			DQ28	56	28
			DQ29	69	29
			DQ30	68	30
			DQ31	70	31
			DQ32	129	32
			DQ33	131	33
			DQ34	141	34
			DQ35	143	35
			DQ36	130	36
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			DQ38	140	38
			DQ39	142	39
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			DQ42	157	42
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			DQ53	166	53
			DQ54	174	54
			DQ55	176	55
			DQ56	181	56
			DQ57	183	57
			DQ58	191	58
			DQ59	193	59
			DQ60	180	60
			DQ61	192	61
			DQ62	194	62
			DQ63	192	63
0	10	DS#0			
1	27	DS#1			
2	45	DS#2			
3	62	DS#3			
4	137	DS#4			
5	154	DS#5			
6	171	DS#6			
7	188	DS#7			
0	10	DS#0			
1	27	DS#1			
2	45	DS#2			
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4	137	DS#4			
5	154	DS#5			
6	169	DS#6			
7	186	DS#7			

TEST 125

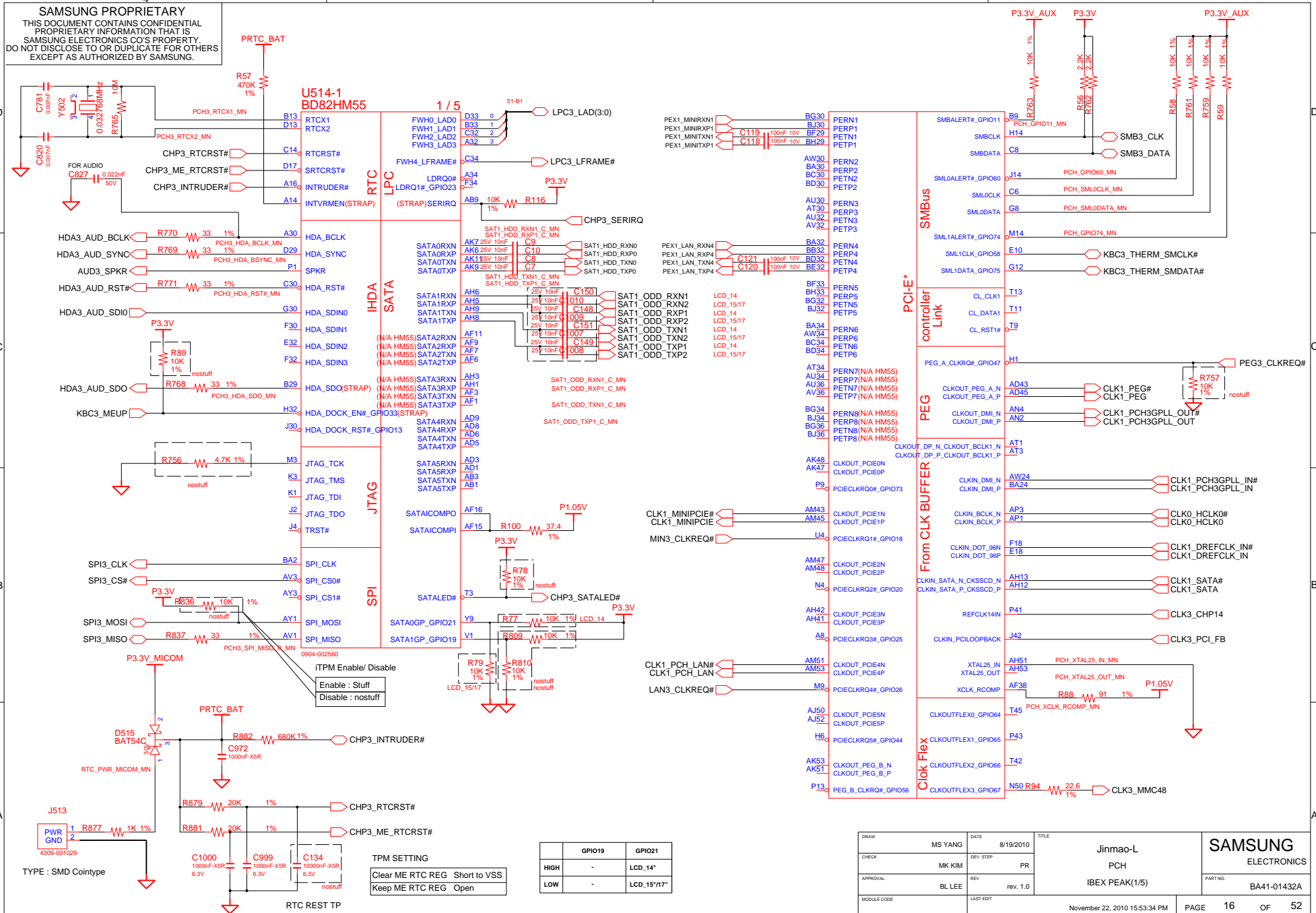
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RESET# 30



COM-22C-015(1996.6.5) REV. 3

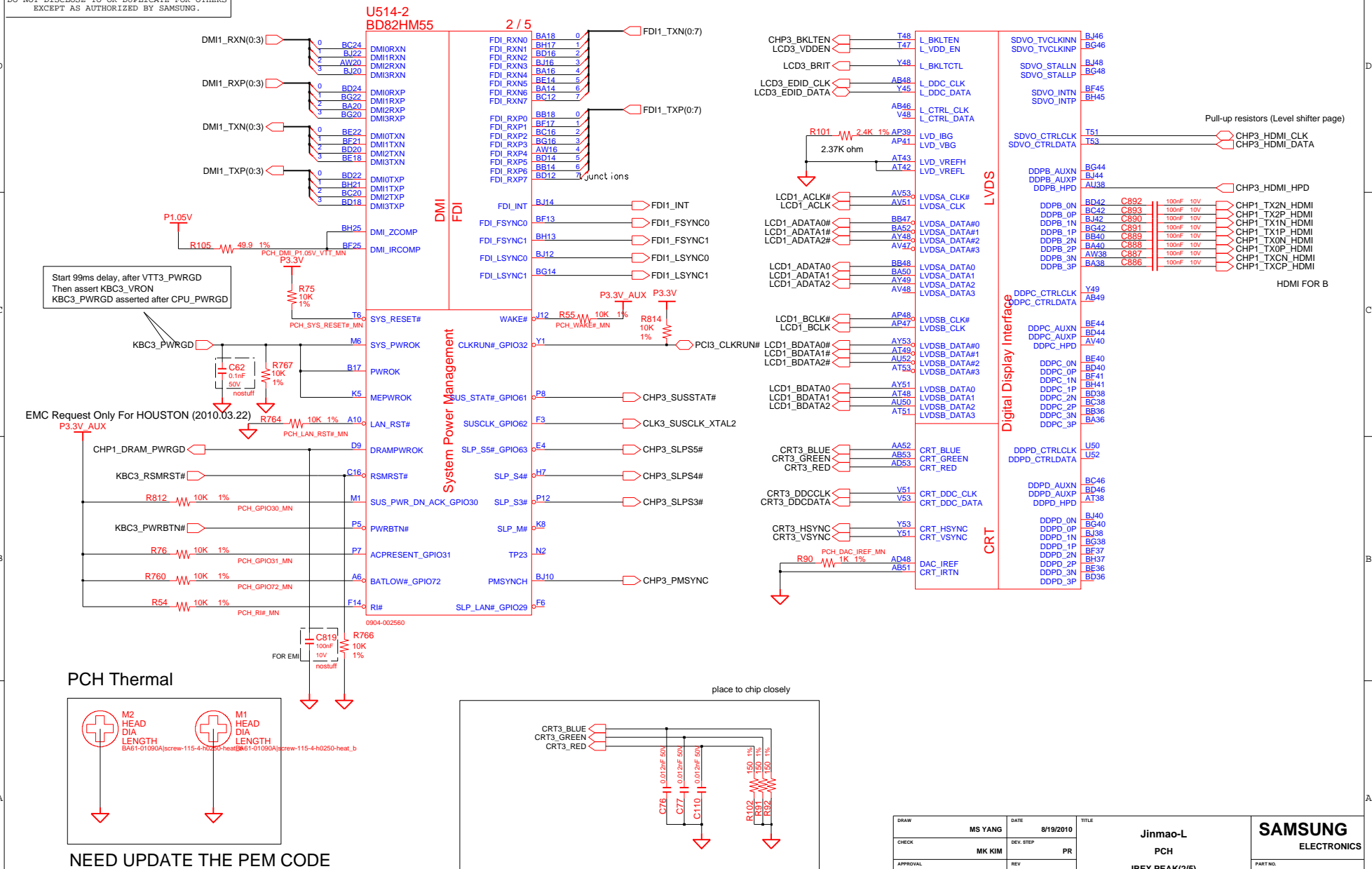
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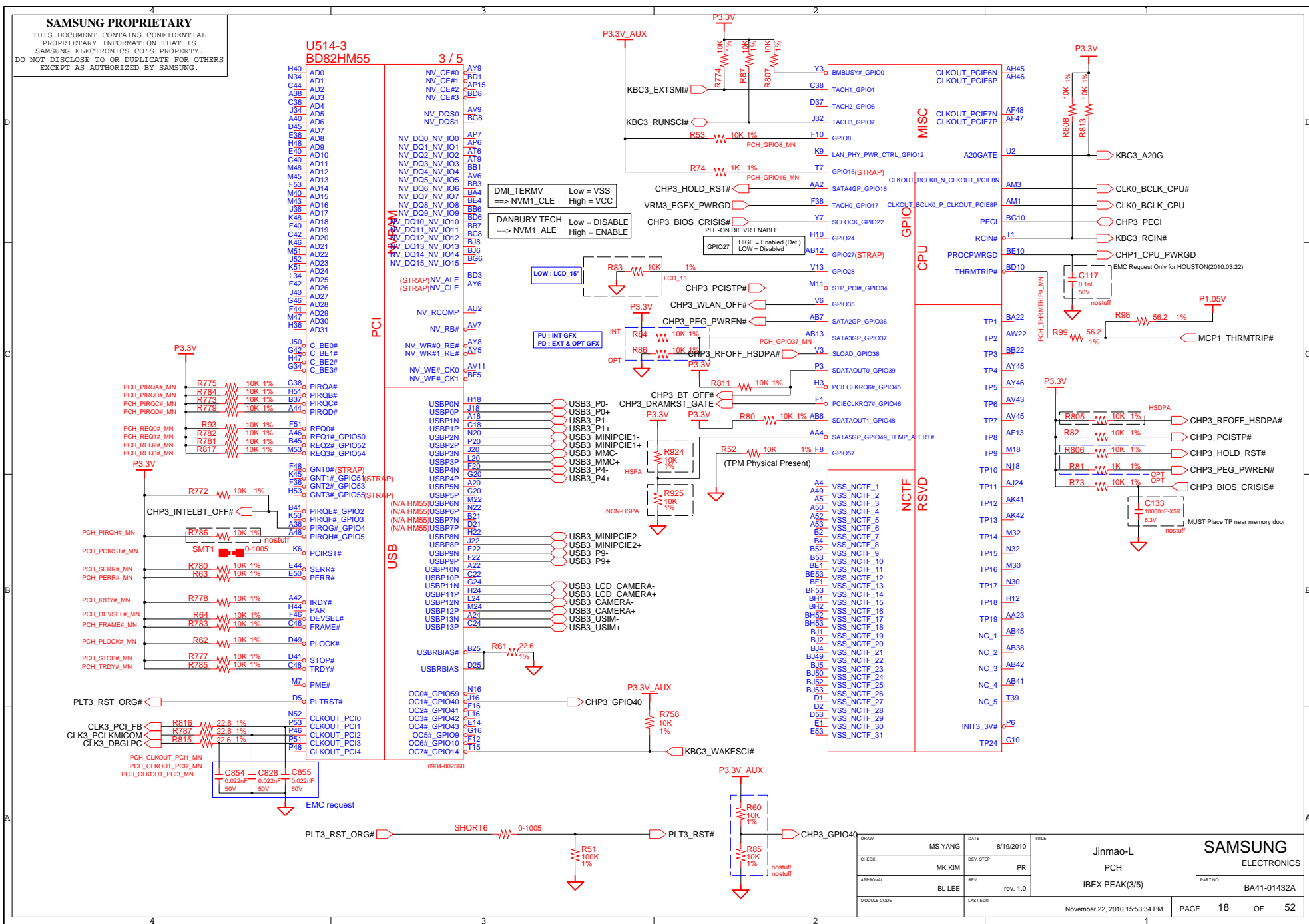


DRAWN	MS YANG	DATE	8/19/2010	Jinmao-L PCH IBEX PEAK(1/5)		<b>SAMSUNG</b> ELECTRONICS	
CHECK	MK KIM	DEV. STEP	PR				
APPROVAL	BL LEE	REV	rev. 1.0	November 22, 2010 15:53:34 PM		PART NO.	BA41-01432A
MODULE CODE		LAST EDIT				PAGE	16

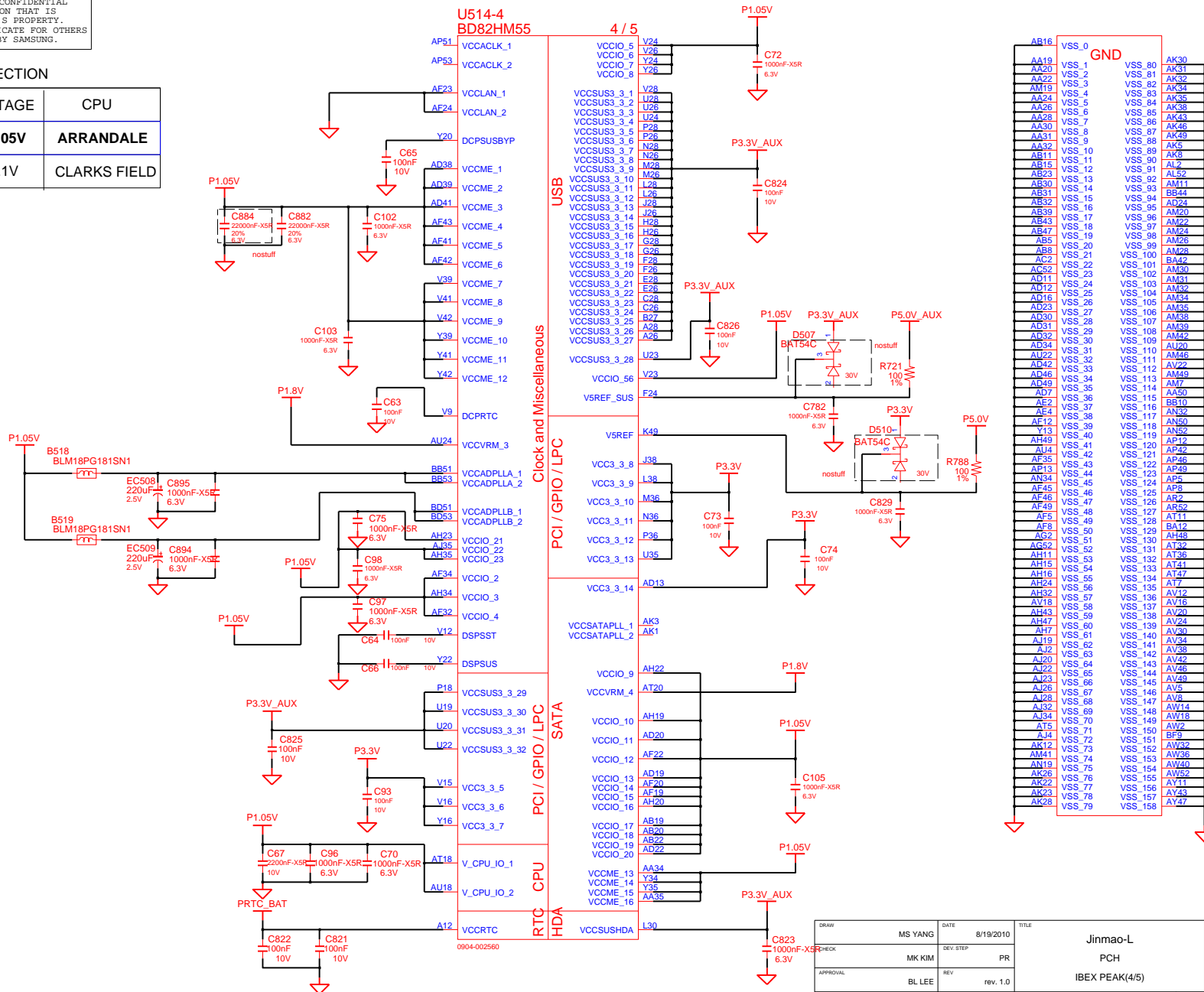


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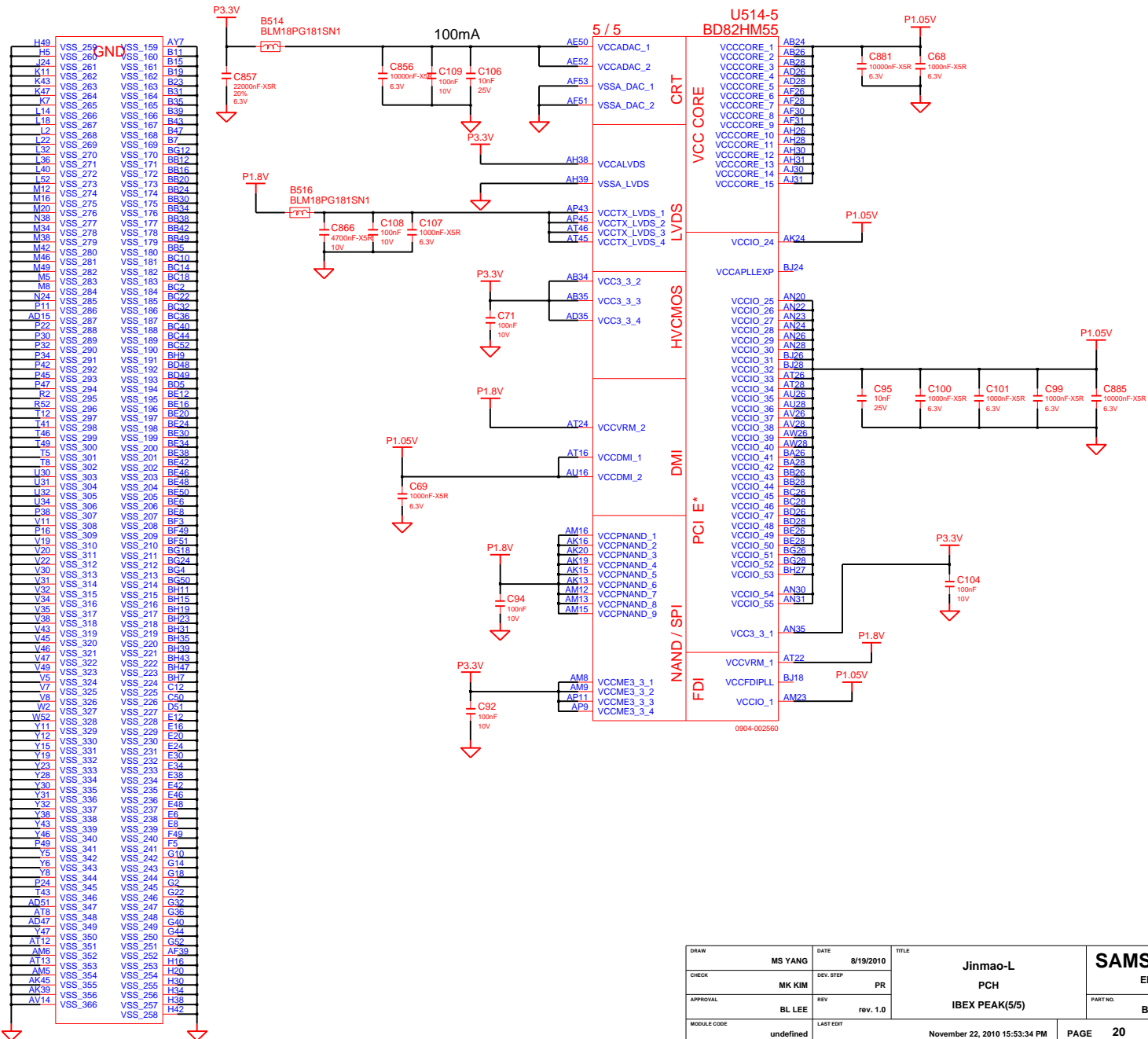


VTT_SEL	VOLTAGE	CPU
1	P1.05V	ARRANDALE
0	P1.1V	CLARKS FIELD



DRAW	MS YANG	DATE	8/19/2010	Jinmao-L PCH IBEX PEAK(4/5)	SAMSUNG ELECTRONICS	
CHECK	MK KIM	DEV. STEP	PR			
APPROVAL	BL LEE	REV	rev. 1.0			
MODULE CODE			LAST EDIT			PAGE
52			November 22, 2010 15:53:34 PM		19	60
				PART NO. BA41-01432A		

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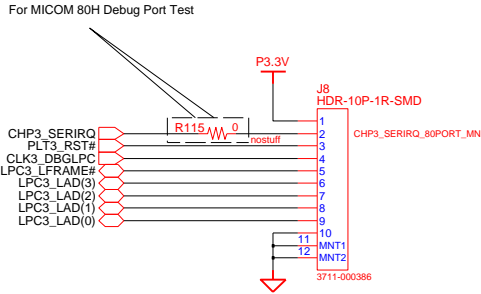
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APPROVAL	BL LEE	REV	REV. 1.0		
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November 22, 2010 15:53:34 PM				PAGE	20
				OF	52

3

2

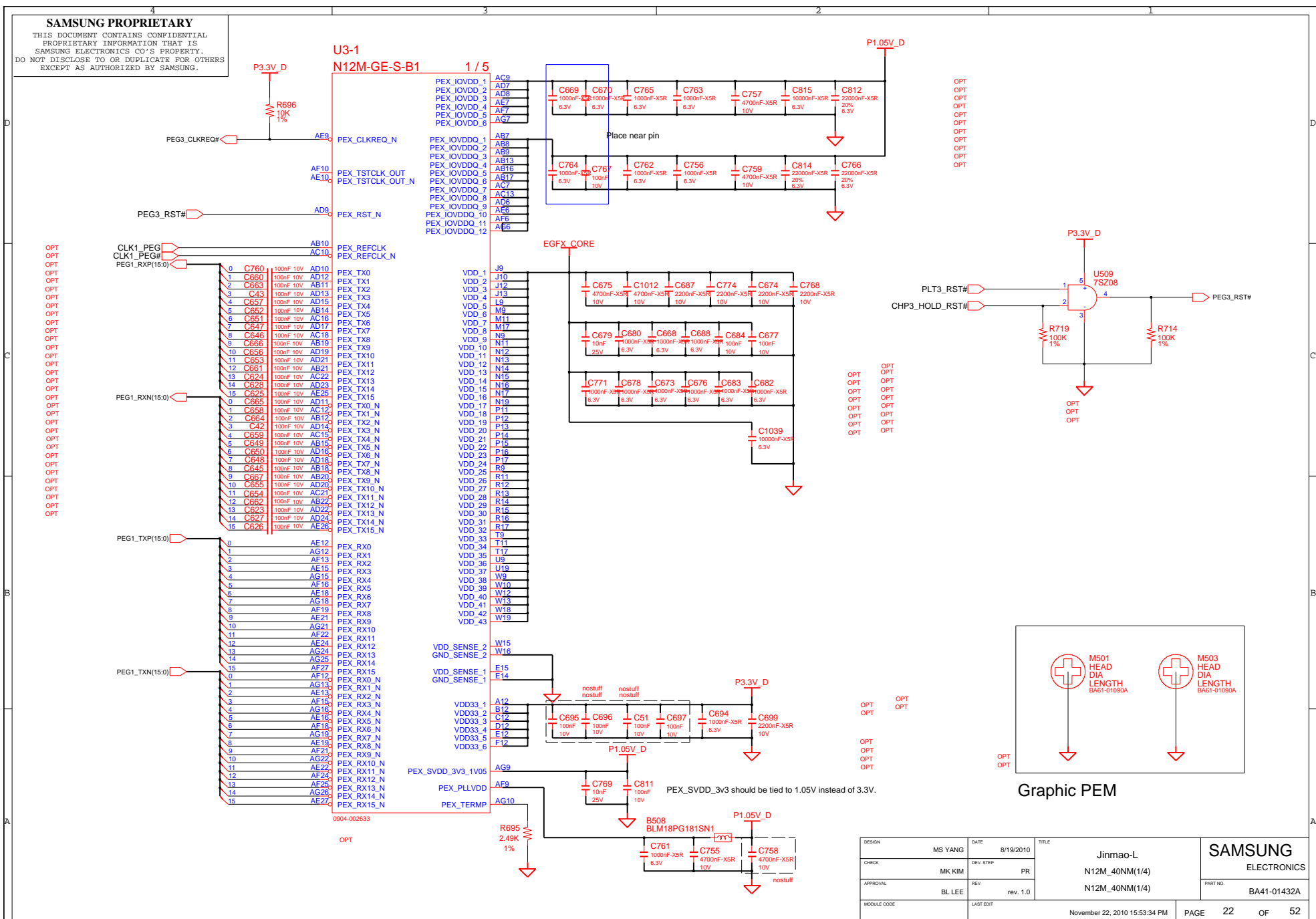
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# 80H PORT DEBUG



DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR	DEBUG PORT		ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0	80H DECODER		PART NO. BA41-01432A
MODULE CODE		LAST EDIT	November 22, 2010 15:53:34 PM	PAGE	21	OF 52

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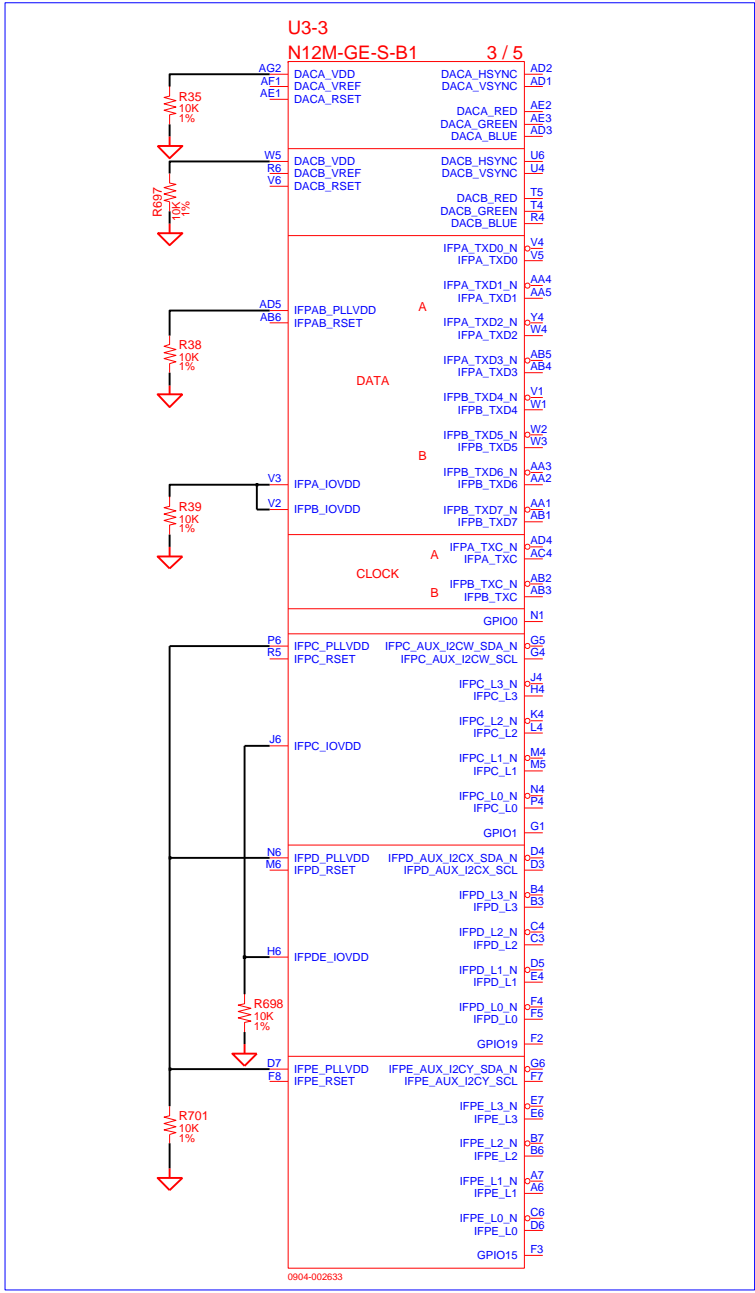


OPT OPT  
OPT OPT  
OPT OPT

COM-22C-015(1996.6.5) REV. 3

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OPT



DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR		N12M_40NM(3/4)	
APPROVAL	BL LEE	REV	rev. 1.0		N12M_40NM(3/4)	
MODULE CODE		LAST EDIT	November 22, 2010 15:53:34 PM	PAGE	24	OF 52



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Pin	Description	Activate
GPIO(0)	General Purpose	NC
GPIO(1)	HPD-C	NC
GPIO(2)	LCD0_BL_PWM	High
GPIO(3)	LCD0_VDD	High
GPIO(4)	LCD0_BL_EN	High
GPIO(5)	GPU VID0	00 0.8V 10 0.95V
GPIO(6)	GPU VID1	01 0.85V 11 1.03V
GPIO(7)	GPU VID2	NC
GPIO(8)	OVERT	LOW
GPIO(9)	ALERT	NC
GPIO(10)	MEM_VREF	NC
GPIO(11)	SLI_SYNC	NC
GPIO(12)	PWR_LEVEL	NC
GPIO(13)	MEM_VID	NC
GPIO(14)	PWR_CTRL1	NC
GPIO(15)	HPD-E	High
GPIO(16)	FAN_PWM	NC
GPIO(17)	Reserved	NC
GPIO(18)	Reserved	NC
GPIO(19)	HPD-D	NC

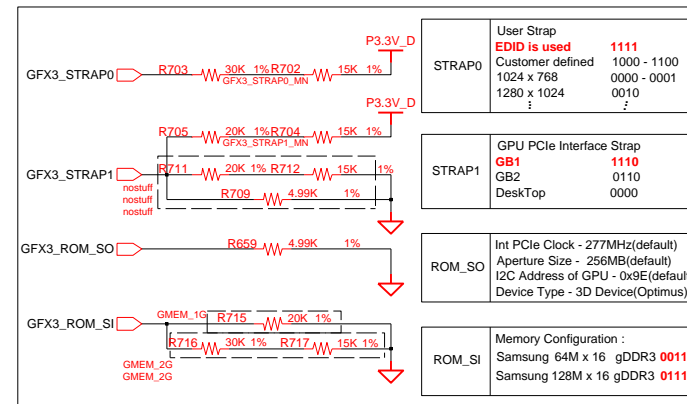
Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	DEVID[4]	VENID	CLK_CFG	PLL_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
STRAP1	PADCFG[3]	PADCFG[2]	PADCFG[1]	PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
Resistor value	PU to VDD	PD to GND	XCLK417 = 0 27MHz	
5K ohm	1000	0000	RAM CFG (SEC)	
10 Kohm	1001	0001	0011 gDDR3 1Gb	
15K ohm	1010	0010	USER[3:0]=1111 for EDID	
20K ohm	1011	0011	PADCFG[3:0]=0110 for NB	
25K ohm	1100	0100		
30K ohm	1101	0101		
35K ohm	1110	0110		
45K ohm	1111	0111		

	Bit3	Bit2	Bit1	Bit0
ROMSO	0	0	0	0
SCLK	1	0	1	0
Si	0	0	1	0
Si	0	1	1	1
Strap2	0	0	0	0
Strap2	0	1	0	1
Strap1	1	1	1	0
Strap0	1	1	1	1

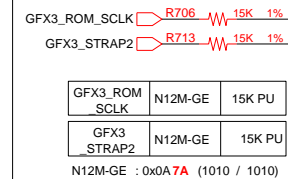
U3-5  
N12M-GE-S-B1

5 / 5

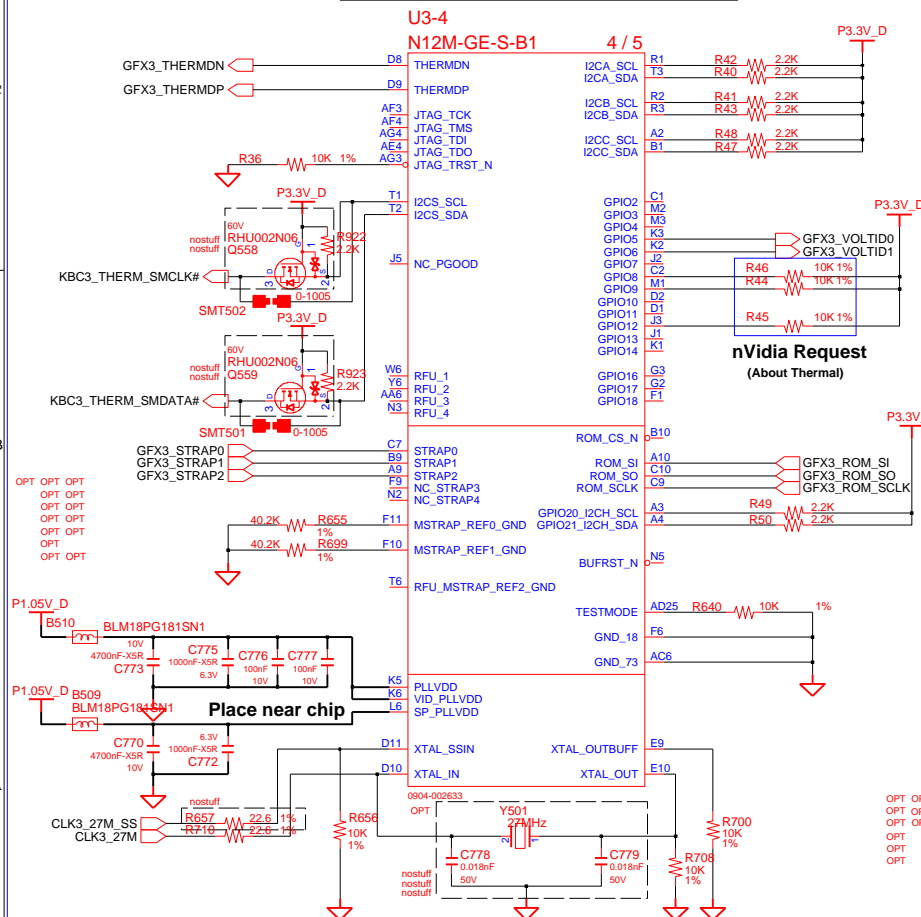
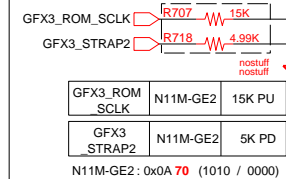
## Function Straps



## Chip Select Straps (N12M-GB1)



## Chip Select Straps (N11M-GB1)



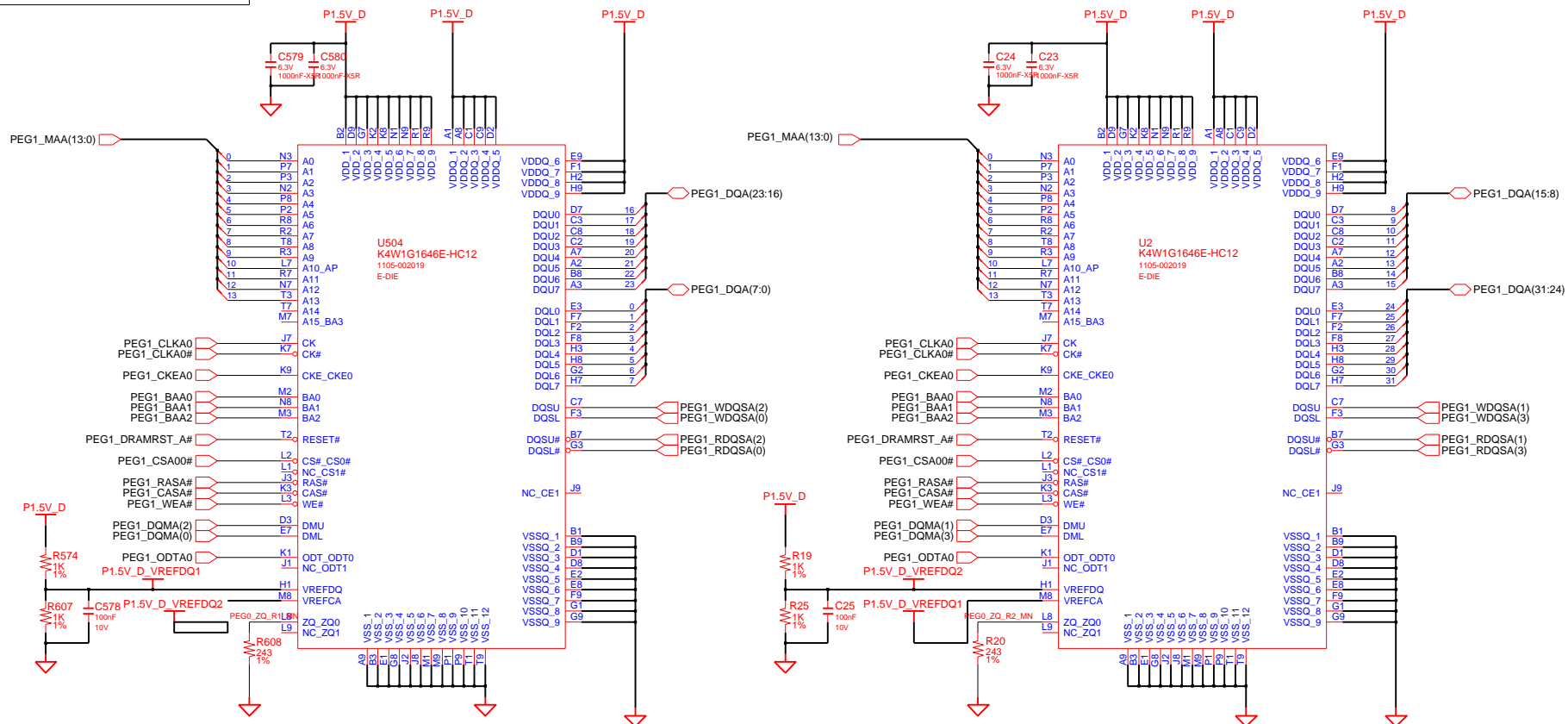
OPT OPT  
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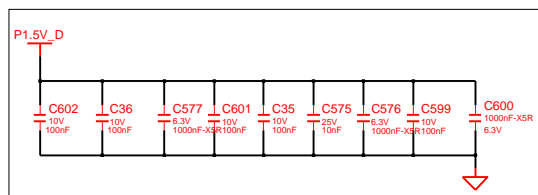
DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR		N12M_40NM(4/4)	
APPROVAL	BL LEE	REV	rev. 1.0		N12M_40NM(4/4)	
MODULE CODE		LAST EDIT				
November 22, 2010 15:53:34 PM						PAGE 25 OF 52

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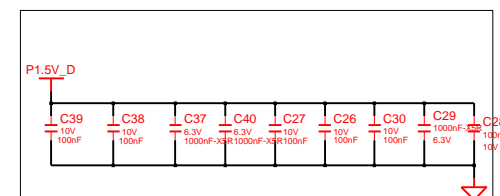
## A-Channel #0



Place near to VDDQ

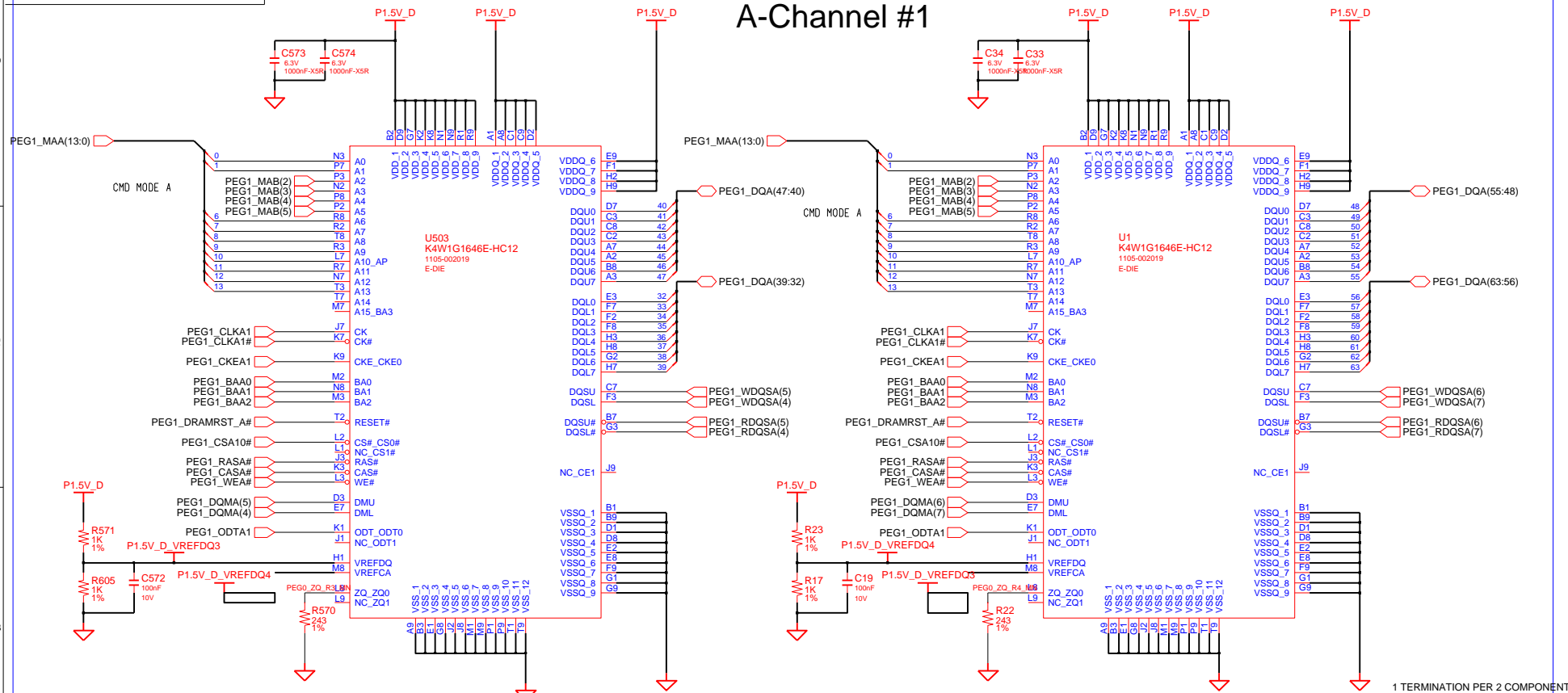


Place near to VDDQ

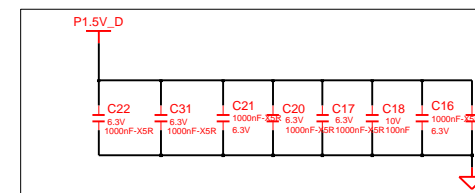
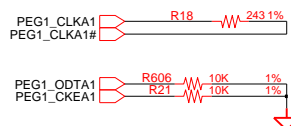
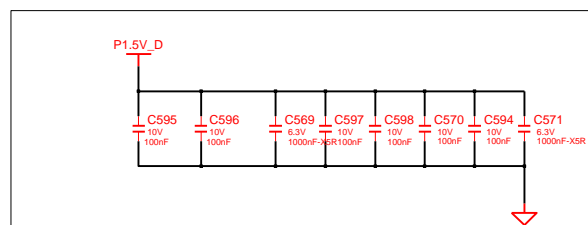


DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG	
CHECK	MK KIM	DEV. STEP	PR	GRAPHIC_MEM A#0		ELECTRONICS	
APPROVAL	BL LEE	REV	rev. 1.0	GRAPHIC_MEM A#0		PART NO.	BA41-01432A
MODULE CODE	LAST EDIT				November 22, 2010 15:53:34 PM	PAGE 26	OF 52

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Place near to VDDQ



1 TERMINATION PER 2 COMPONENT

OPT OPT  
OPT OPT  
OPT OPT  
OPT OPT  
OPT OPT  
OPT OPT  
OPT OPT  
OPT OPT

DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L		
CHECK	MK KIM	DEV. STEP	PR	GRAPHIC_MEM A#1			
APPROVAL	BL LEE	REV	rev. 1.0	GRAPHIC_MEM A#1		PART NO.	BA41-01432A
MODULE CODE	LAST EDIT			November 22, 2010 15:53:34 PM		PAGE	27 OF 52

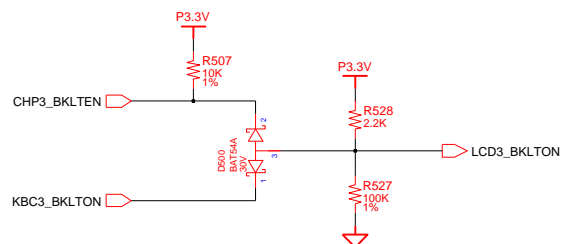
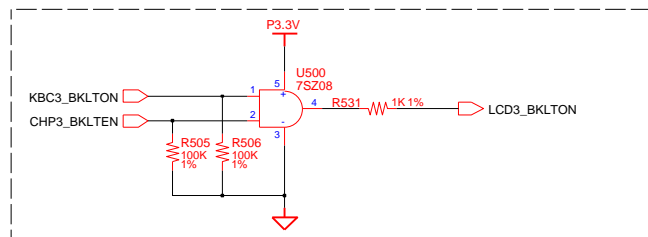
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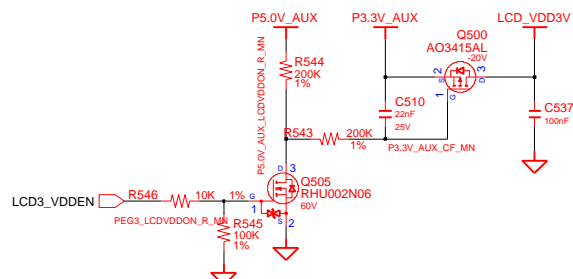
# LVDS LOGIC

## 1Ch. LCD Connector + CAMERA

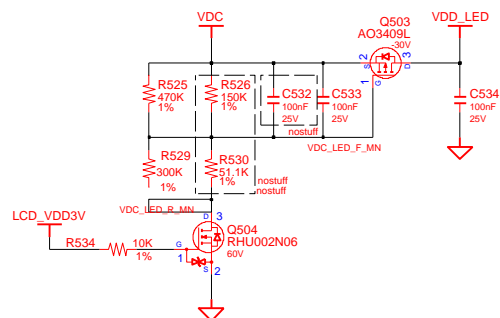
### Backlight On



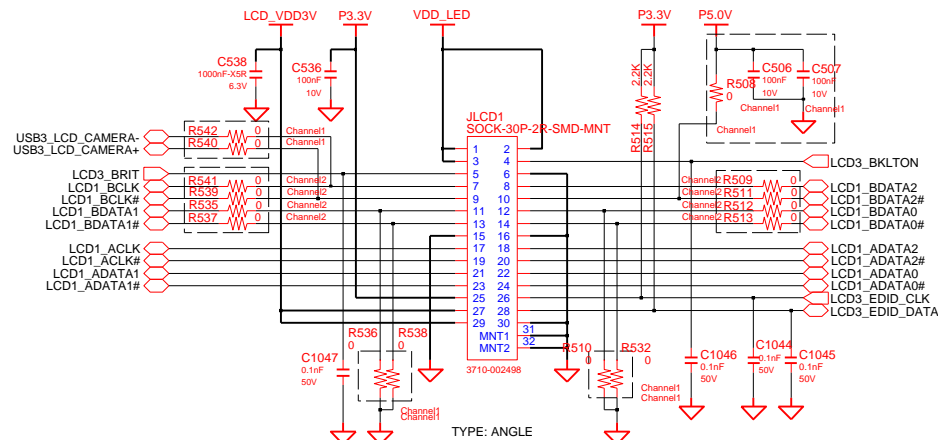
### LCD Power



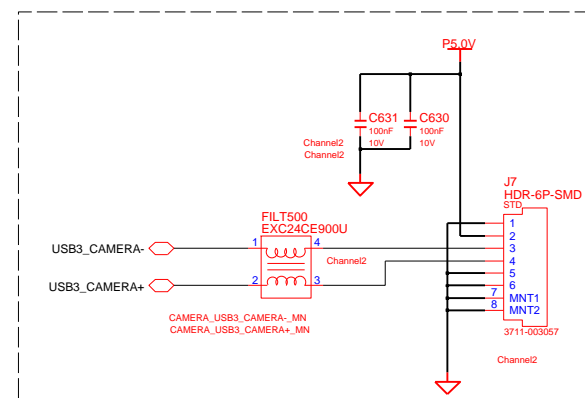
### LED Power



NOTE : Place R20 close to connector to minimize stub



## CAMERA CONN FOR 2ch LVDS

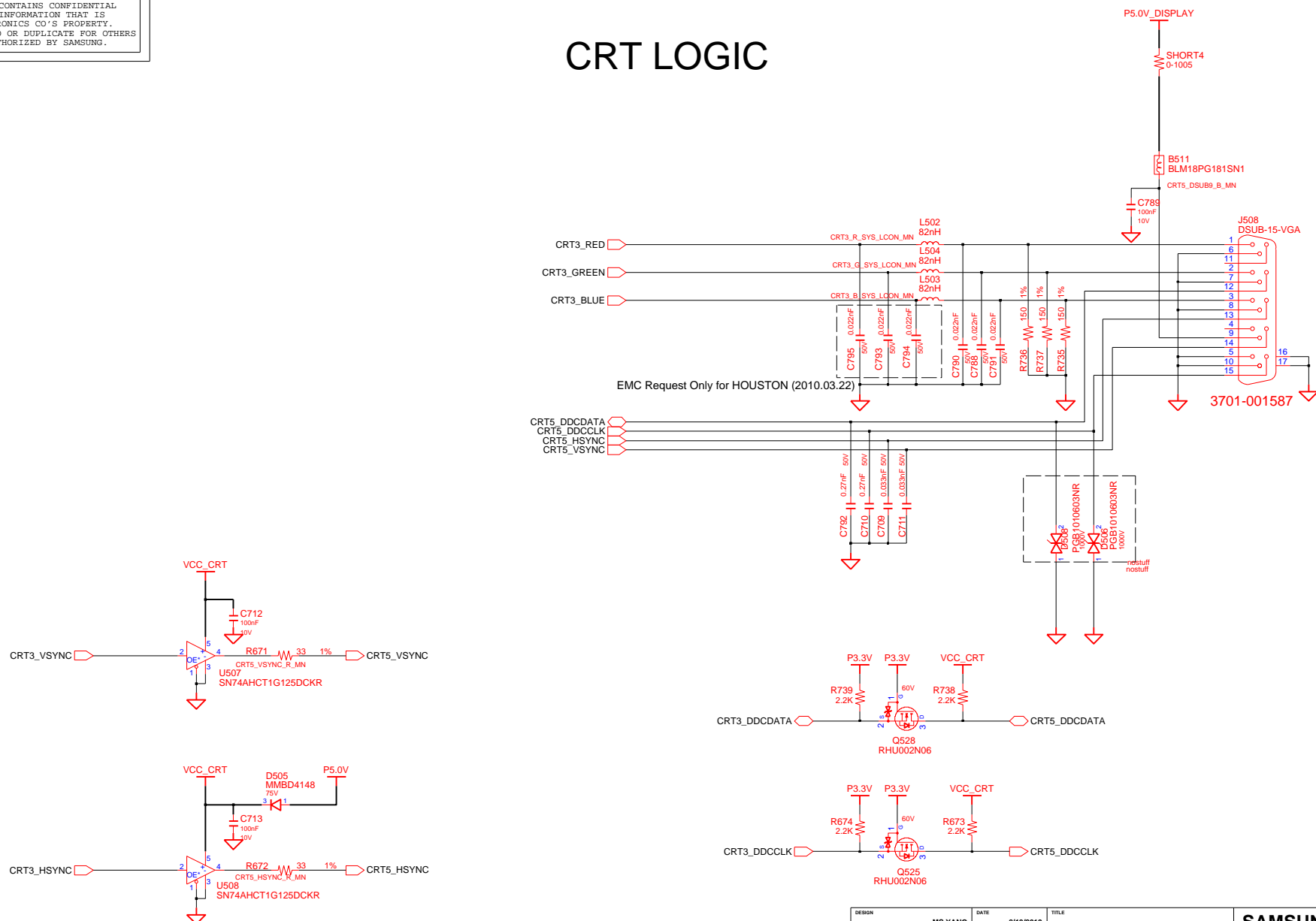


DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR		GRAPHICS_IF	ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0		LVDS	PART NO.
MODULE CODE		LAST EDIT				BA41-01432A
November 22, 2010 15:53:34 PM						PAGE 28 OF 52

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## CRT LOGIC



DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR		GRAPHICS_IF	
APPROVAL	BL LEE	REV	rev. 1.0		CRT	
MODULE CODE		LAST EDIT				
November 22, 2010 15:53:34 PM						PAGE 29 OF 52

After checking, Houston need to use CMC for each signal.  
(EMC request at 2010.04.15)



FOR ASM1442

PC1	PC0
00	8dB
01	4dB
10	12dB
11	0dB

CG_2	CG_1	CG_0	Swing	Pre-amp	Slew rate
0	0	0	450mV	0dB	0dB
0	0	1	490mV	0dB	-3dB
0	1	0	450mV	0dB	-3dB
0	1	1	460mV	0dB	-4dB
1	0	0	340mV	0dB	0dB
1	0	1	400mV	2dB	0dB
1	1	0	400mV	2dB	0dB
1	1	1	420mV	0dB	0dB

HDMI Level Shifter	REXT(Pin6)	PC1_CG0(Pin3)	PC1_CG1(Pin4)	RT_ENG2_CG2(Pin10)	NC_EQ_0(Pin34)	NC_EQ_1(Pin35)	Note	4-6 CODE
PS8101	499 phm	stuff	nostuff	nostuff	NC	NC		1006-001427
ASM1442	3.4K(3.24~3.3K)	nostuff	nostuff	nostuff	nostuff	nostuff	Internal PU/PD exist CGs nostuff is 450mV swing	1006-001471

FOR ASM1442

EQ_1	EQ_0	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB

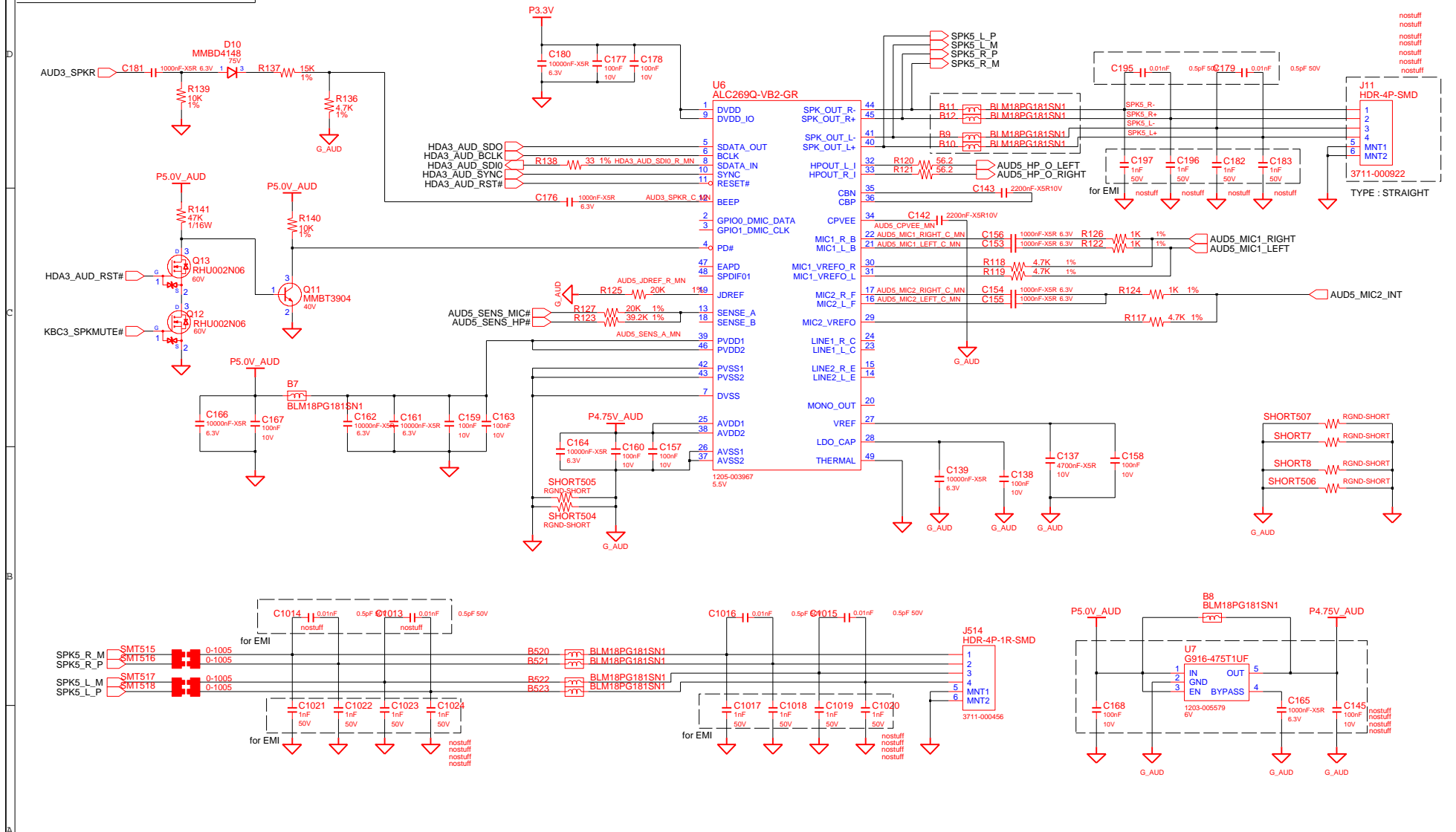
	Internal Default Value
maxSize	1000
minSize	100
initialCapacity	100
loadFactor	0.75
trimToSize	false
allowRandomAccess	true
serialVersionUID	-6847921510945569476L

DESIGN	MS YANG	DATE	8/19/2010	Jinmao-L GRAPHICS_IF HDMI	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR		
APPROVAL	BL LEE	REV	rev. 1.0		
MODULE CODE		LAST EDIT			
November 22, 2010 15:53:34 PM					PAGE 30 OF 52

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# HD AUDIO

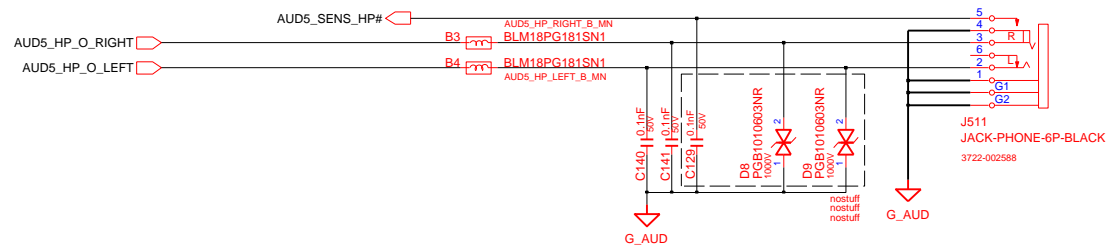


DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L
CHECK	MK KIM	DEV. STEP	PR		HDA_CODEC SUB
APPROVAL	BL LEE	REV	rev. 1.0		AUDIO CODEC ALC269 SUB
MODULE CODE		LAST EDIT			
				November 22, 2010 15:53:34 PM	PAGE 31 OF 52

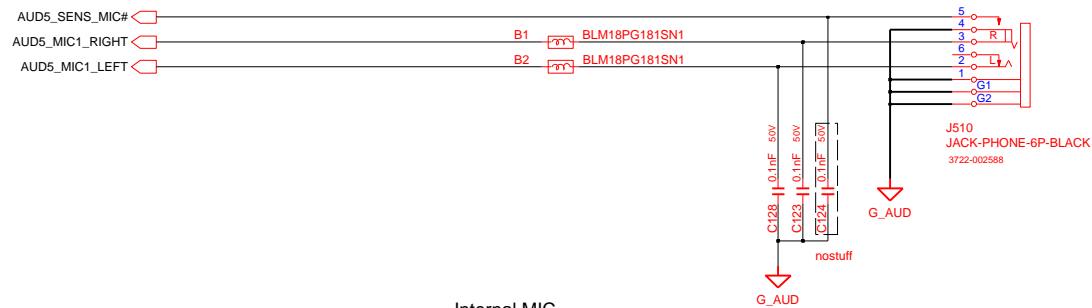
**SAMSUNG**  
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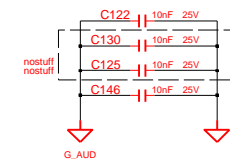
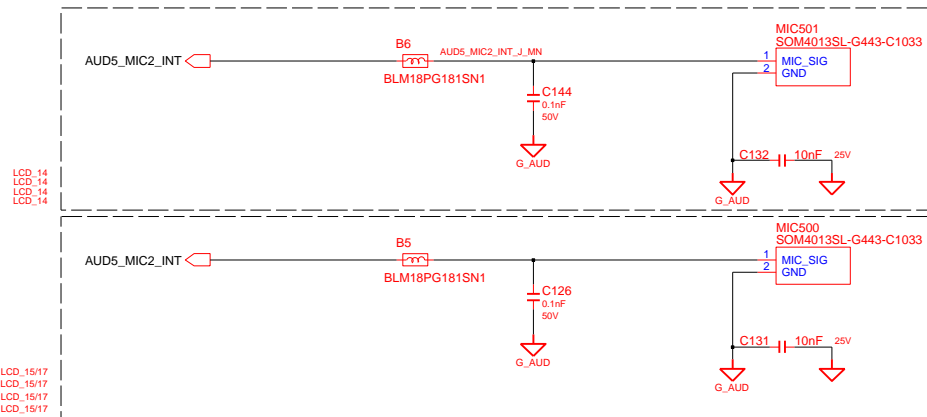
## HEADPHONE



## MIC JACK



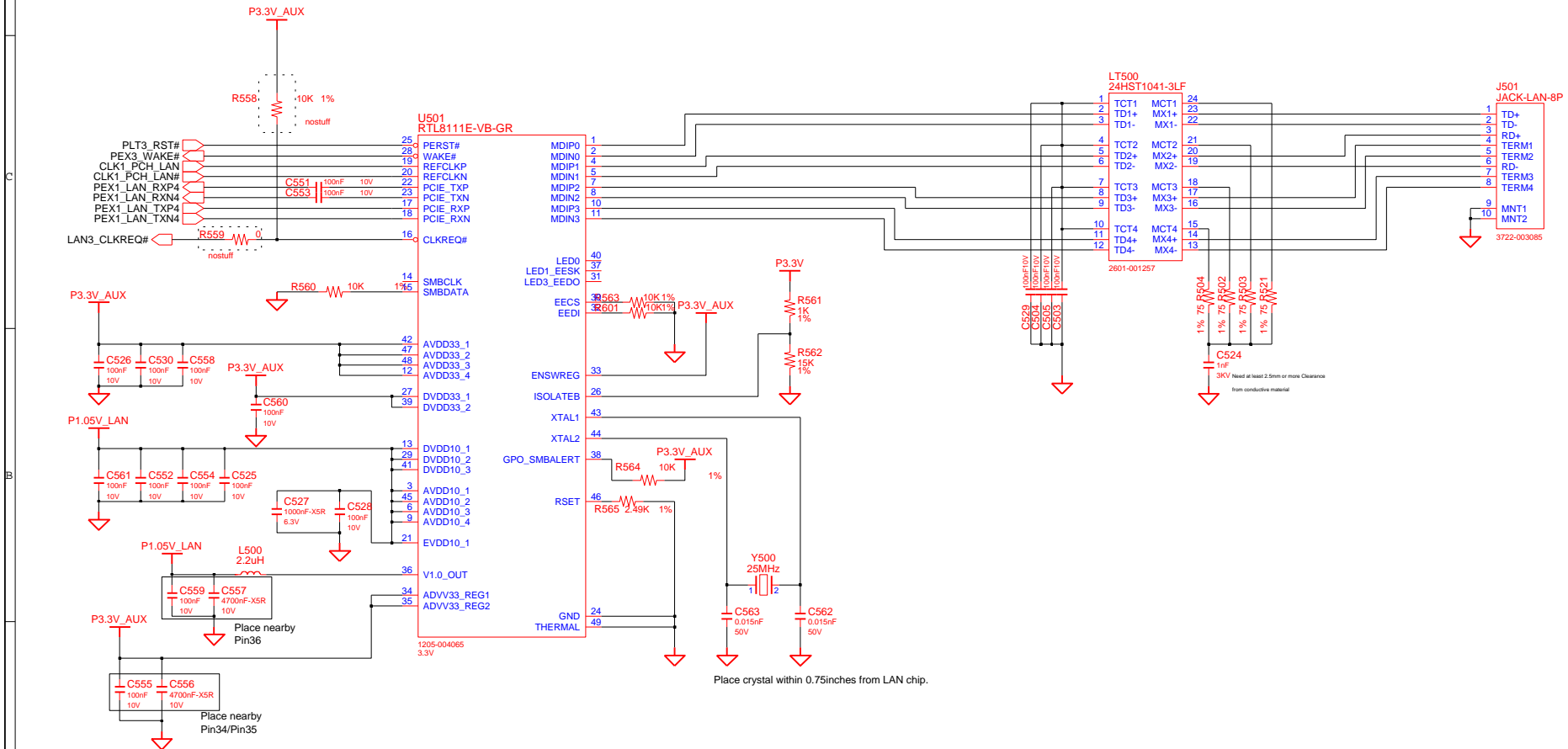
## Internal MIC



DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR		HDA_CODEC & LED SUB	
APPROVAL	BL LEE	REV	rev. 1.0		AUDIO JACK & LED SUB	
MODULE CODE		LAST EDIT				
				November 22, 2010 15:53:34 PM	PAGE 32 OF 52	PART NO. BA41-01432A



# Reatek RTL8111E

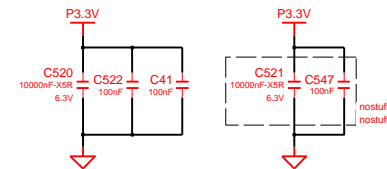
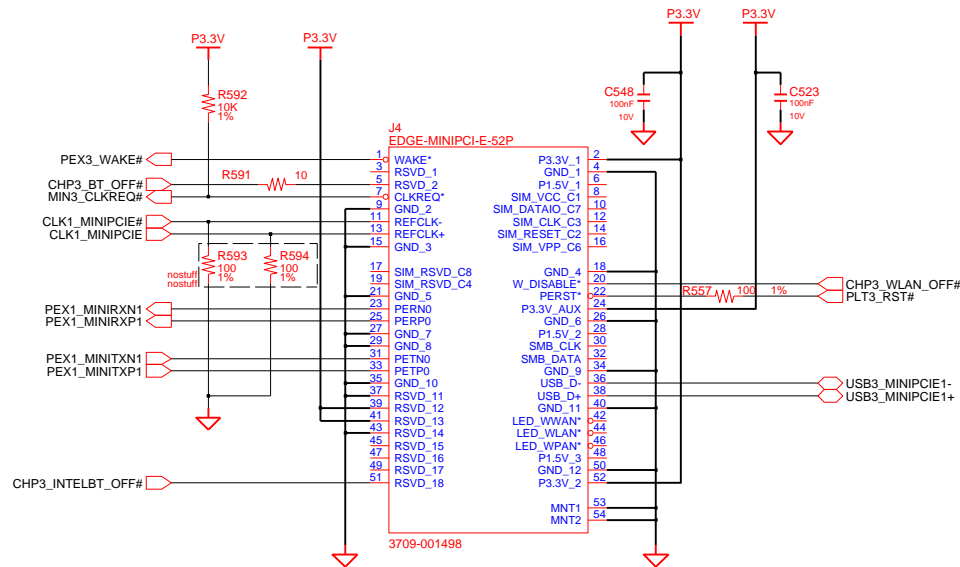


DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR	LAN	LAN	ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0	LAN_Realtek_RTL8111	PART NO.	BA41-01432A
MODULE CODE		LAST EDIT		November 22, 2010 15:53:34 PM	PAGE	33 OF 52

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## WLAN

Height : 4.0mm



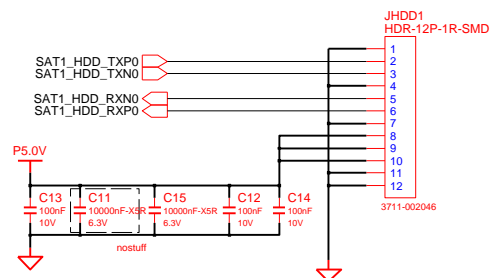
DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR	WLAN	WLAN	
APPROVAL	BL LEE	REV	rev. 1.0	WLAN	WLAN	
MODULE CODE		LAST EDIT				PART NO. BA41-01432A
				November 22, 2010 15:53:34 PM	PAGE 34 OF 52	

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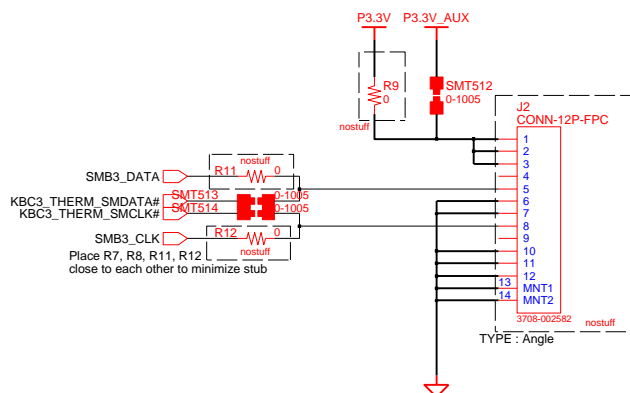
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## SATA HDD CONN

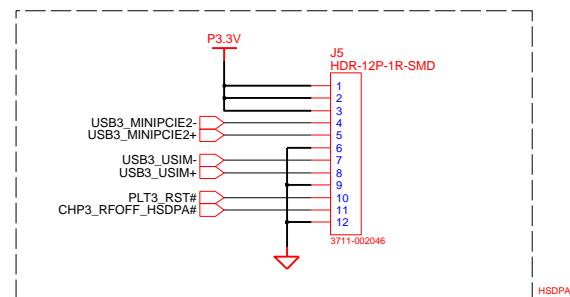
Cable Connector Type



## FOR IR

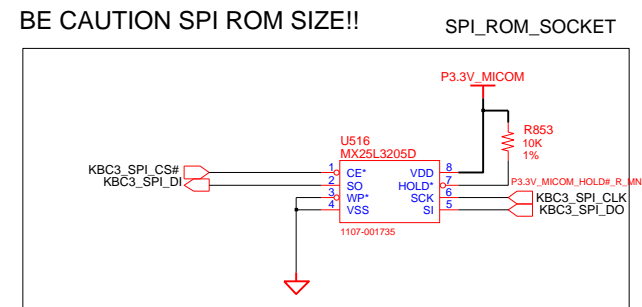


## MAIN to HSDPA SUB



DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR		SATA HDD & IR	ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0		SATA HDD & IR	PART NO.
MODULE CODE		LAST EDIT	November 22, 2010 15:53:34 PM			BA41-01432A
				PAGE	35	OF 52

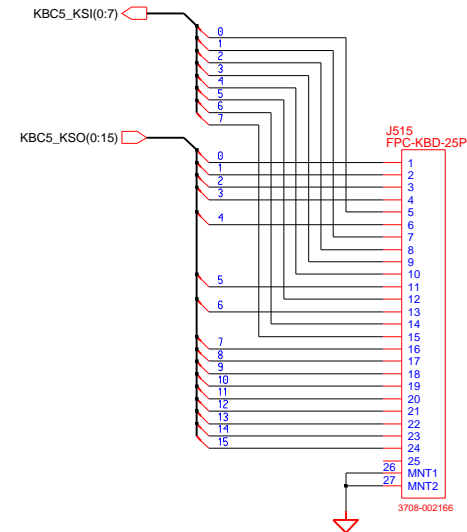
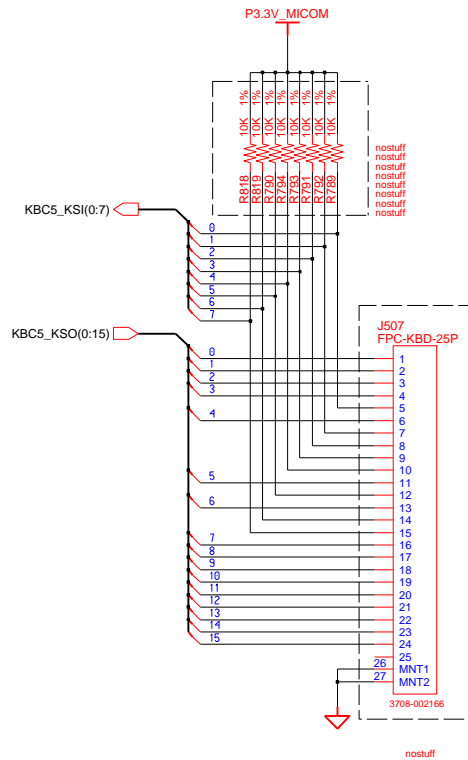
## MAIN BOARD (MICOM)



COM-22C-015(1996.6.5) REV. 3

# Micom Glue Logic

## KEYBOARD



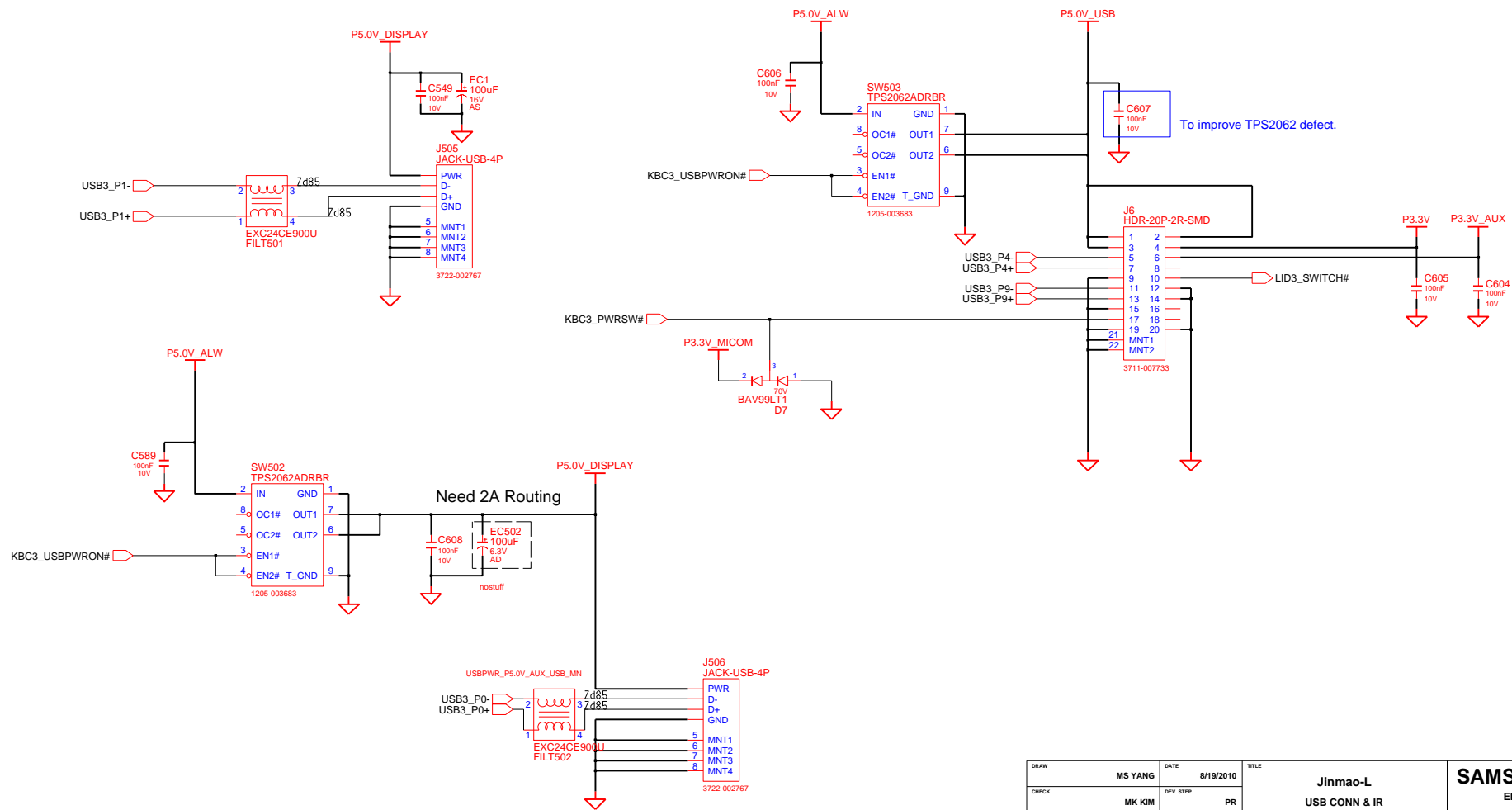
DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR	MICOM GLUE LOGIC		ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0	MICOM GLUE LOGIC	PART NO.	BA41-01432A
MODULE CODE	LAST EDIT				November 22, 2010 15:53:34 PM	PAGE 37 OF 52

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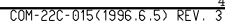
## POWER S/W SUB B'D CONNECTOR

### MAIN to SUB



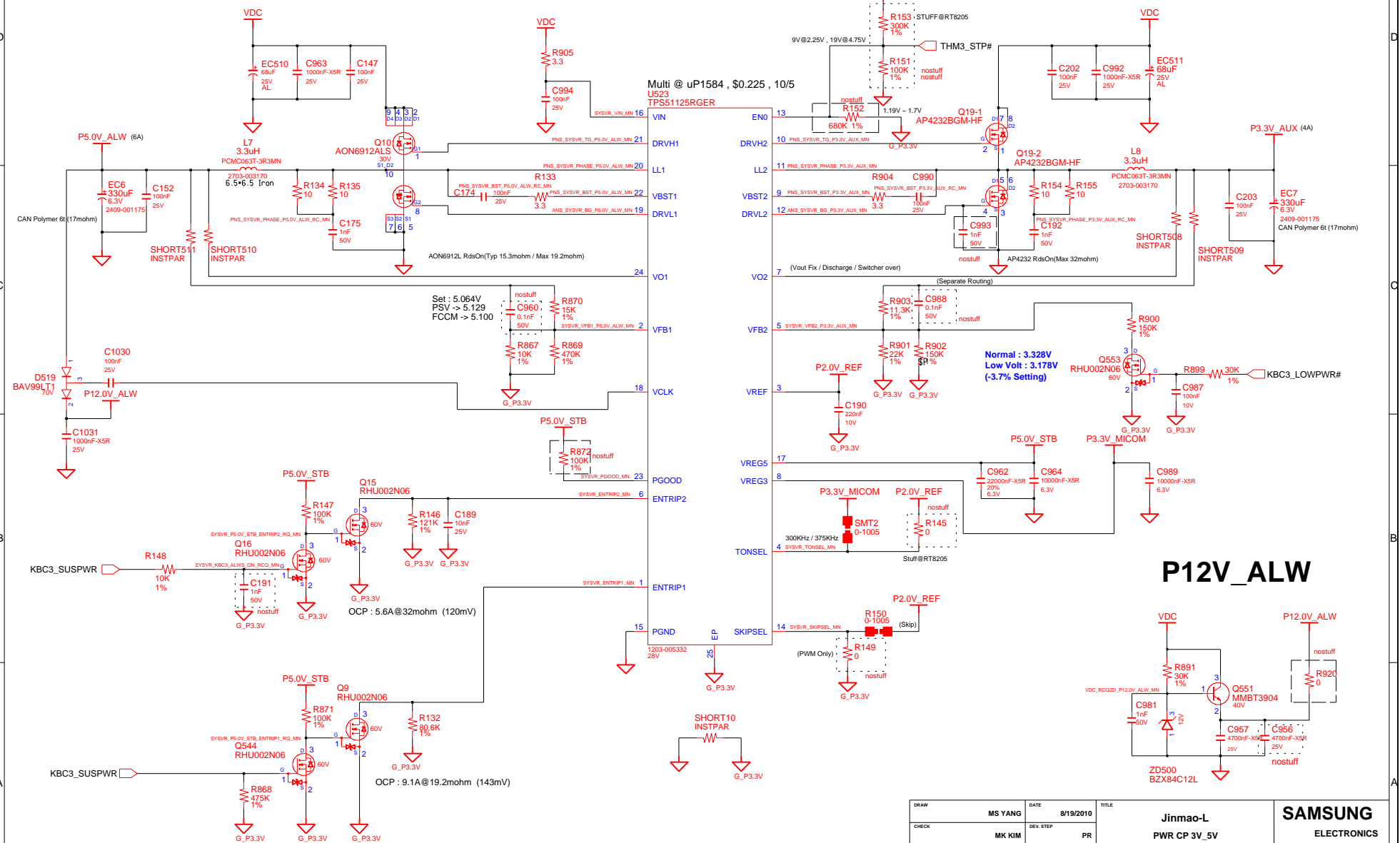
DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR	USB CONN & IR		
APPROVAL	BL LEE	REV	rev. 1.0	USB & IR		
MODULE CODE		LAST EDIT		November 22, 2010 15:53:34 PM	PAGE 38 OF 52	PART NO. BA41-01432A

## CHARGER & POWER MANAGEMENT



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## P3.3V\_AUX & P5.0V\_AUX



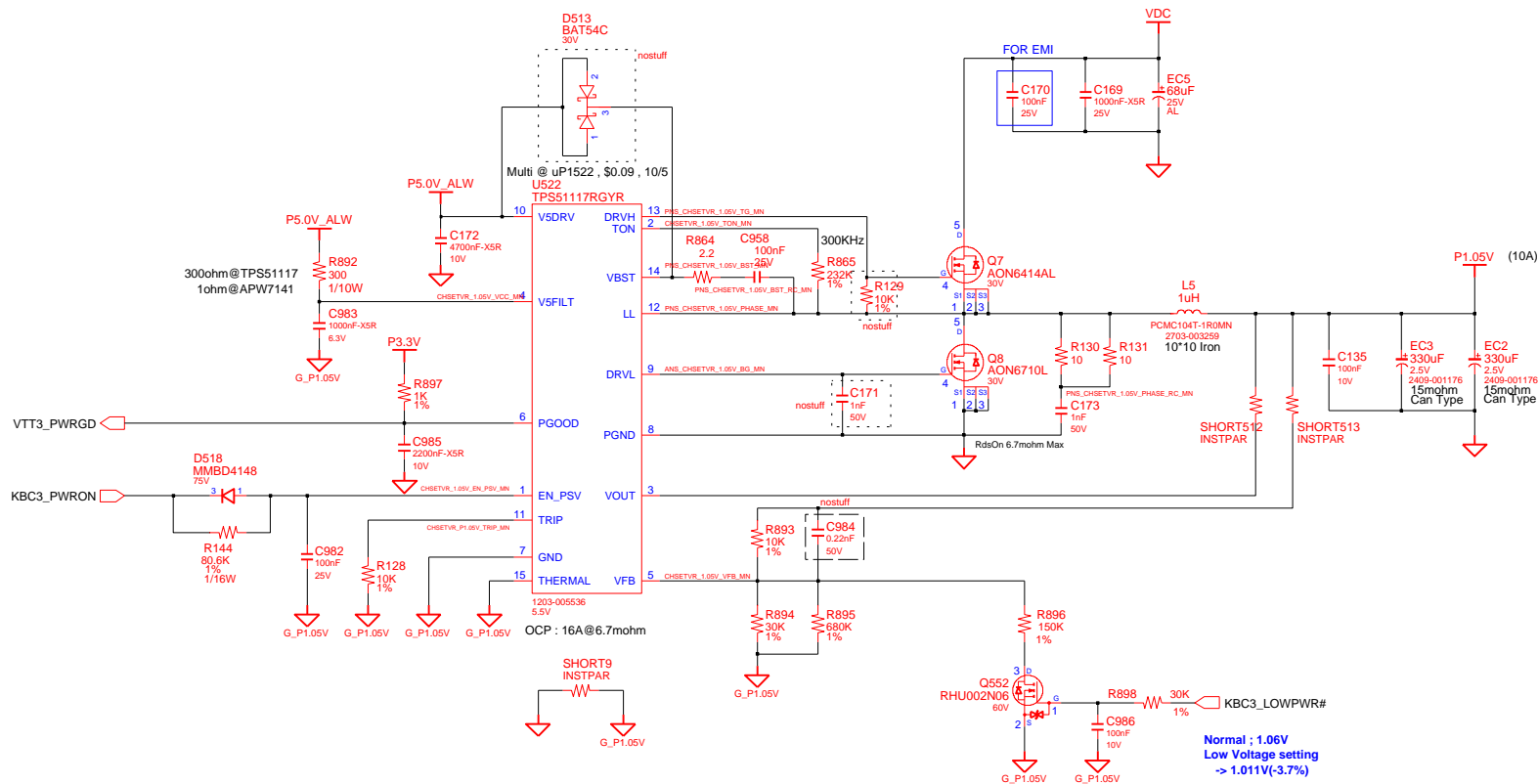
DRAW	MS YANG	DATE	8/19/2010	TITLE		SAMSUNG ELECTRONICS	
CHECK	MK KIM	DEV. STEP	PR	Jinmao-L PWR CP 3V_5V			
APPROVAL	BL LEE	REV	rev. 1.0	P3.3V_AUX / P5.0V_AUX			
				PART NO.		BA41-01432A	
MODULE CODE	undefined	LAST EDIT		November 22, 2010 15:53:34 PM		PAGE	40 OF 52



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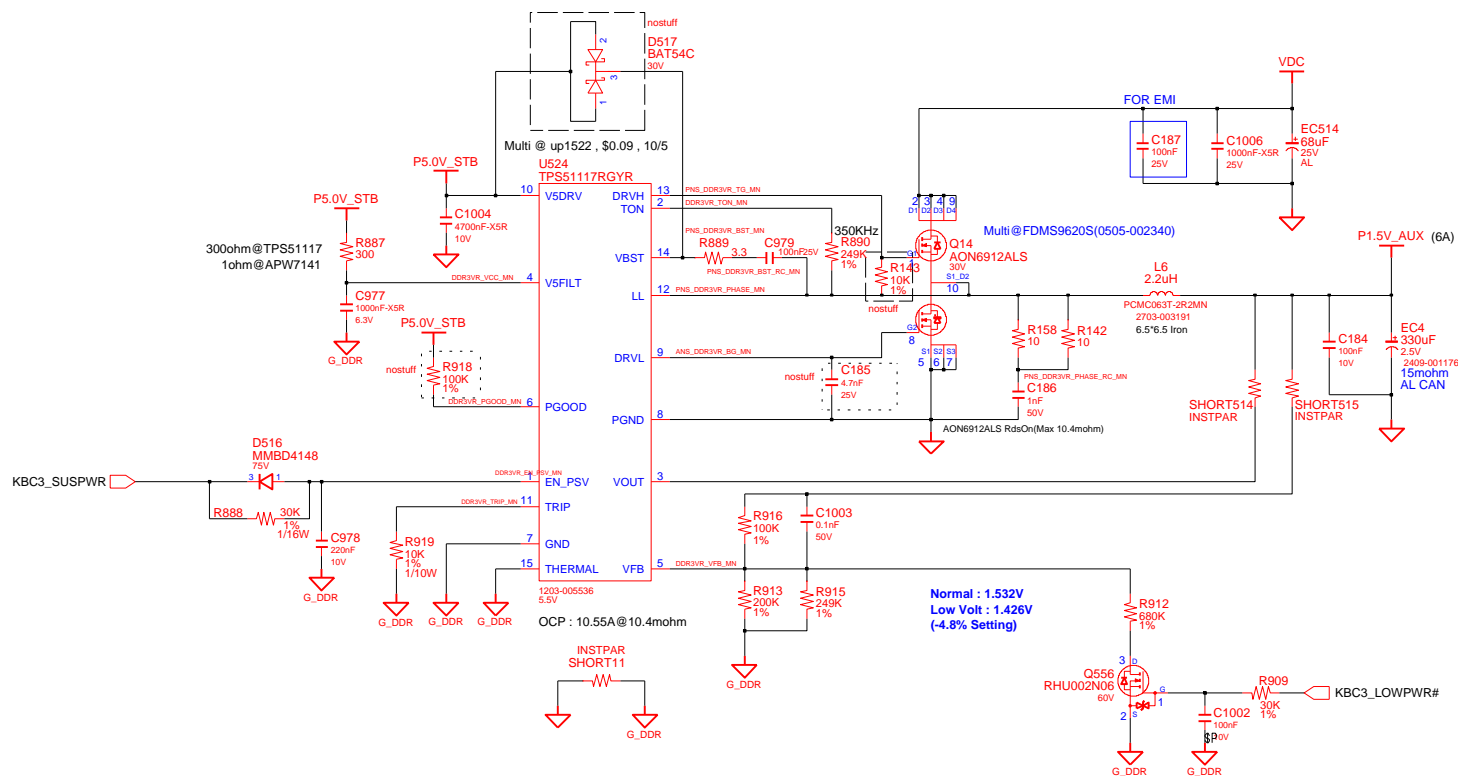
## CHIPSET POWER(P1.05V)



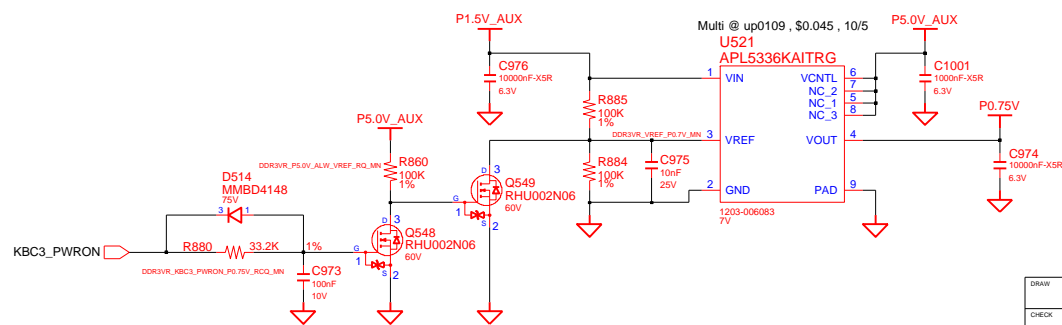
DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR		P1.05V	
APPROVAL	BL LEE	REV	rev. 1.0		TI TPS51117R	
MODULE CODE		LAST EDIT				PART NO. BA41-01432A
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## DDR3 Power



## DDR3 VTT(0.75V)



DRAW	MS YANG	DATE	8/19/2010	Jinmao-L PWR MEMORY RT8207	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR		
APPROVAL	BL LEE	REV	rev. 1.0		
MODULE CODE		LAST EDIT			
undefined		November 22, 2010 15:53:34 PM			PAGE 42 OF 52

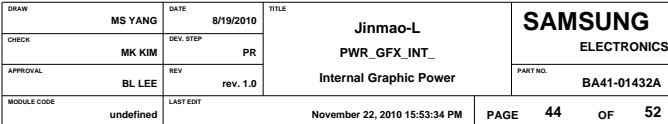
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VID[5:3] @ IMON CPU Gain  
100 @ 50A (ARD)  
101 @ 60A (CFD)

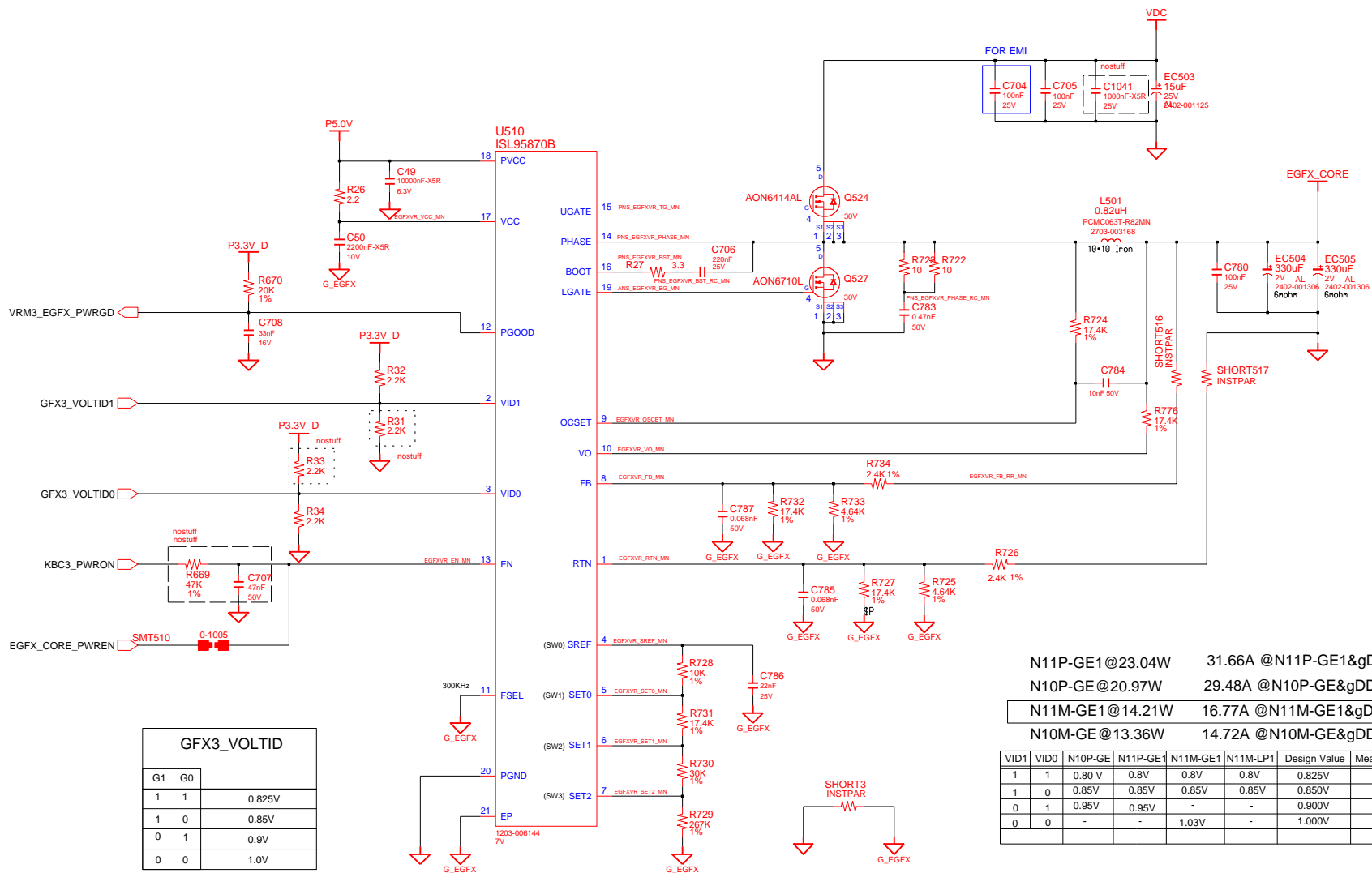
[illegible]

DRAW	MS YANG	DATE	8/19/2010	TITLE  Jinmao-L  PWR_CPU_MV_ISL62882  CPU VRM	SAMSUNG ELECTRONICS		
CHECK	MK KIM	DEV. STEP	PR		PART NO.  BA41-01432A		
APPROVAL	BL LEE	REV	rev. 1.0				
MODULE CODE	undefined	LAST EDIT	November 22, 2010 15:53:34 PM			PAGE	43

## Internal GFX Core Power



## External GFX Core Power



N10M-GE@13.36W	14.72A @N10M-GE&qDDR3
----------------	-----------------------

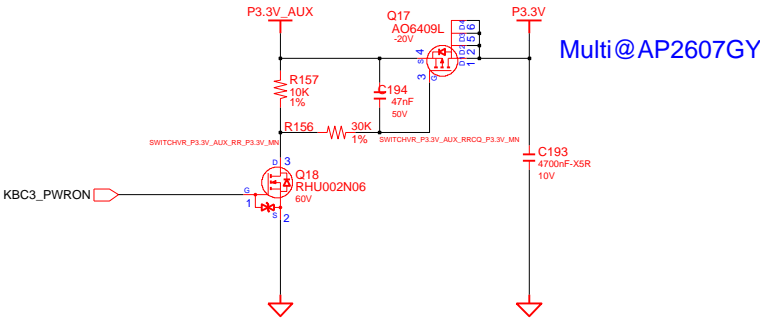
VID1	VID0	N10P-GE	N11P-GE	N11M-GE1	N11M-LP1	Design Value	Measured Value
1	1	0.80 V	0.8V	0.8V	0.8V	0.825V	
1	0	0.85V	0.85V	0.85V	0.85V	0.850V	
0	1	0.95V	0.95V	-	-	0.900V	
0	0	-	-	1.03V	-	1.000V	

DESIGN	MS YANG	DATE	8/19/2010	Jinmao-L PWR_GFX_MV_EXT External Graphic Power	SAMSUNG ELECTRONICS			
CHECK	MK KIM	DEV. STEP	PR					
APPROVAL	BL LEE	REV	REV. 1.0		PART NO.	BA41-01432A		
MODULE CODE	LAST EDIT				November 22, 2010 15:53:34 PM	PAGE	45	OF

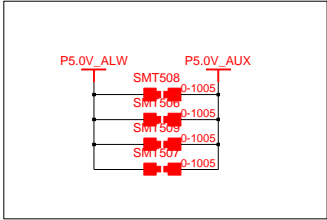
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# Switched Power

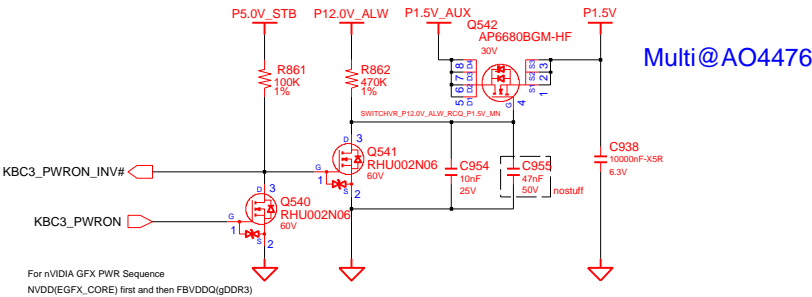
## Switched Power On (P3.3V)



## P5.0V\_AUX

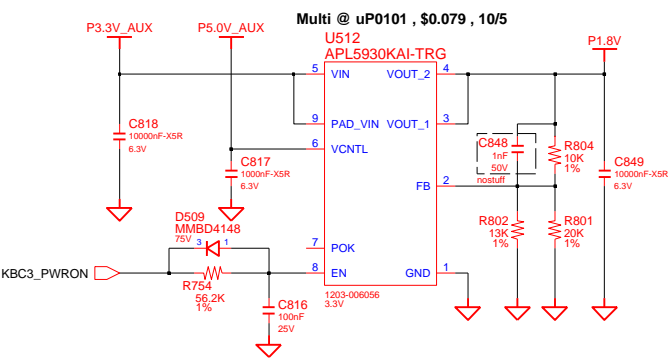


## Switched Power On (P1.5V)

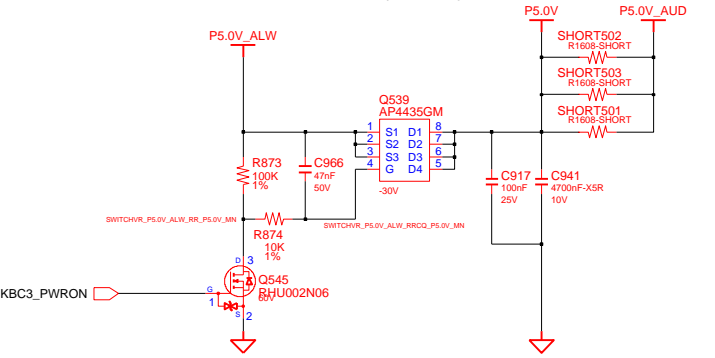


For nVidia GFX PWR Sequence  
NVDD(EGFX\_CORE) first and then FBVDDQ(gDDR3)

## P1.8V(LDO)



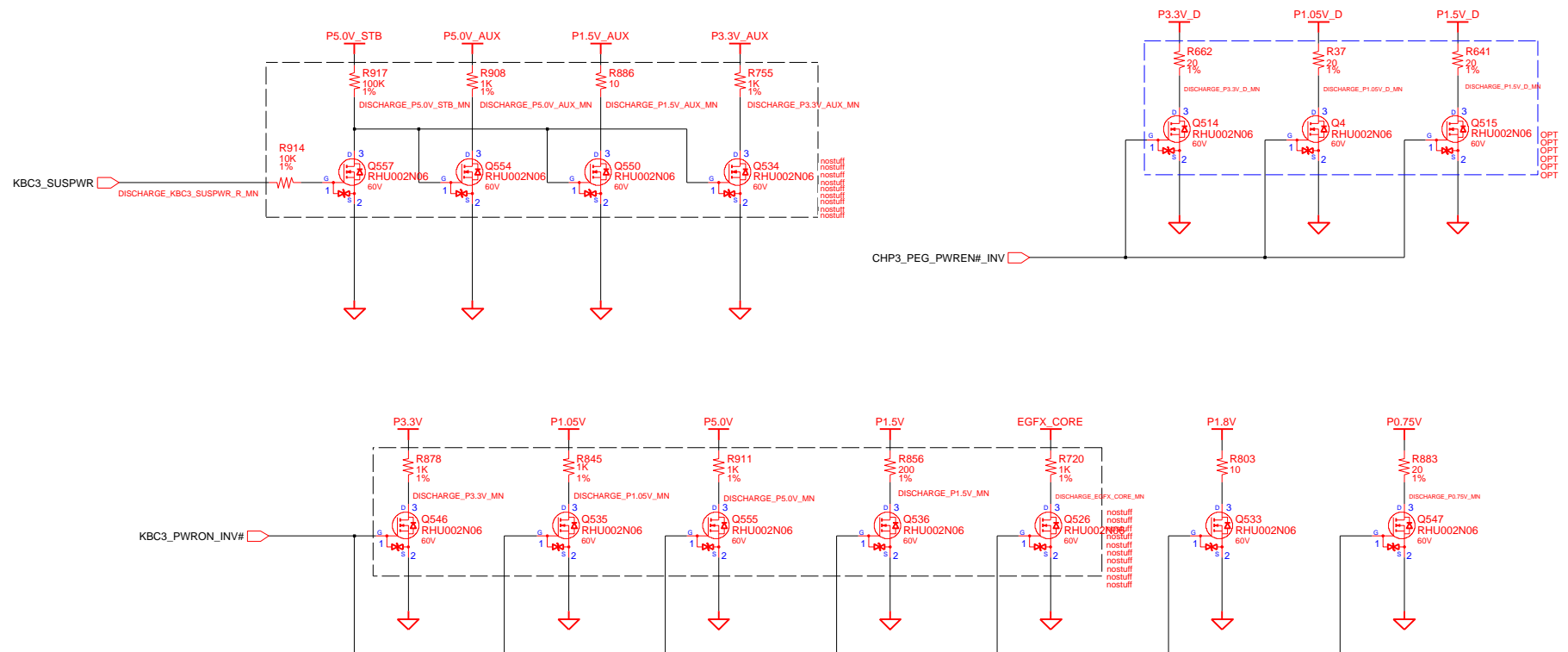
## Switched Power On (P5.0V)



DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG
CHECK	MK KIM	DEV. STEP	PR	PWR_MV_SWITCHED	ELECTRONICS	
APPROVAL	BL LEE	REV	rev. 1.0	SWITCHED POWER	PART NO.	BA41-01432A
MODULE CODE		LAST EDIT		November 22, 2010 15:53:34 PM	PAGE	46 OF 52

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# POWER DISCHARGER

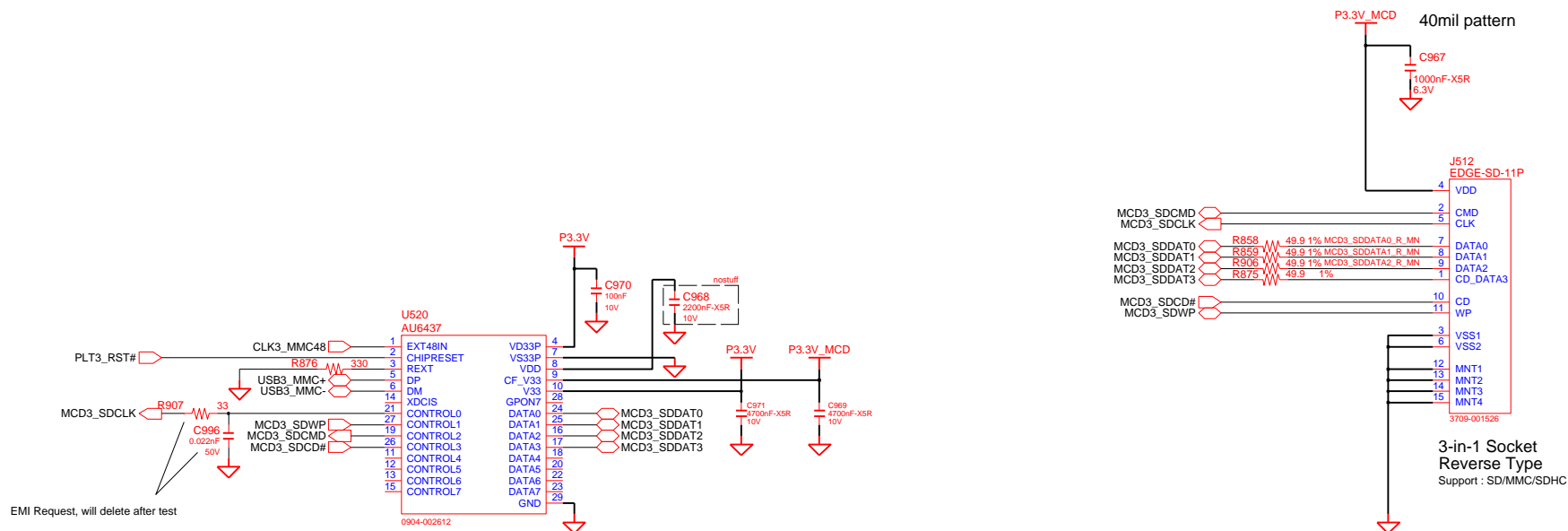


DRAW	MS YANG	DATE	8/19/2010	Jinmao-L PWR_MV_DISCHARGER DISCHARGING LOGIC		SAMSUNG ELECTRONICS PART NO. BA41-01432A	
CHECK	MK KIM	DEV. STEP	PR				
APPROVAL	BL LEE	REV	rev. 1.0				
MODULE CODE	undefined	LAST EDIT	November 22, 2010 15:53:34 PM			PAGE	47 OF 52

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# AU6437 (4-in-1)



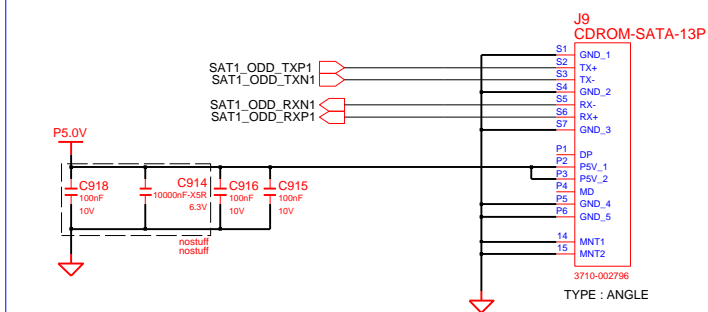
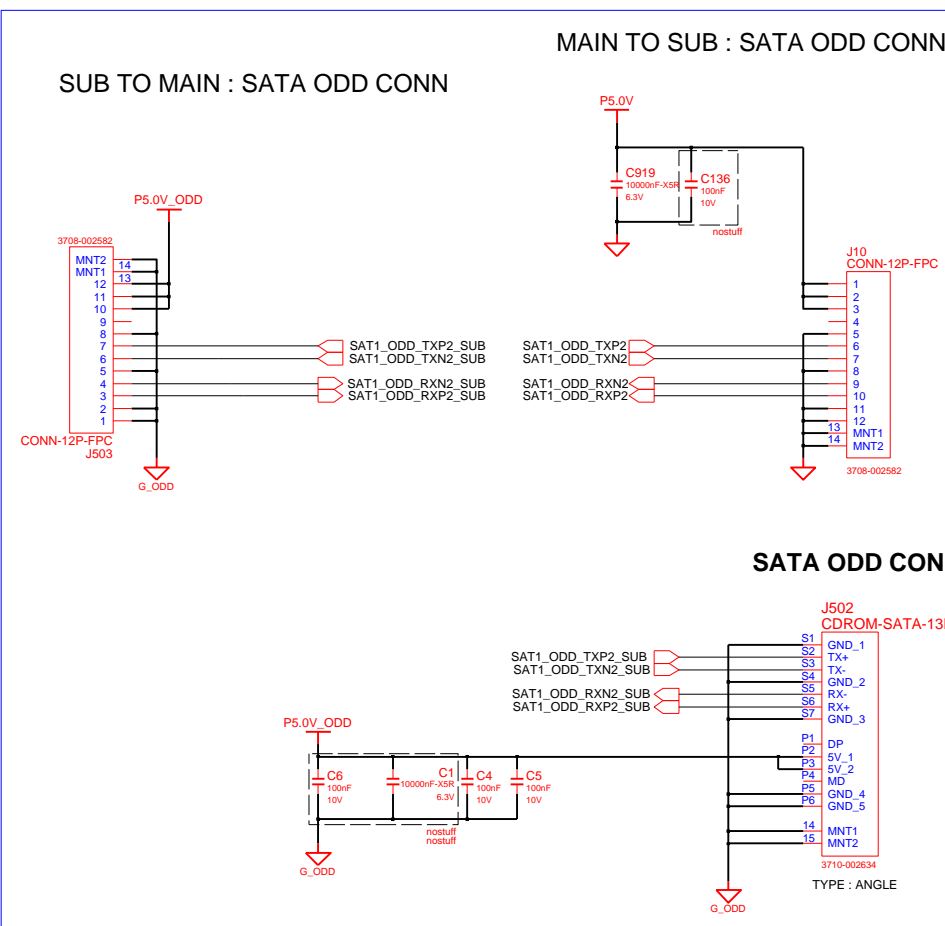
DESIGN	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR	AU 6437	AU 6437	
APPROVAL	BL LEE	REV	rev. 1.0	AU 6437		
MODULE CODE		LAST EDIT	November 22, 2010 15:53:34 PM	PAGE	48	OF 52



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# SATA ODD SUB BOARD

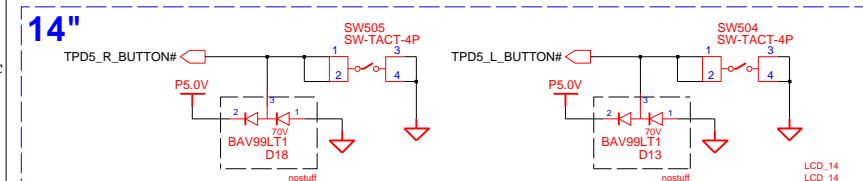
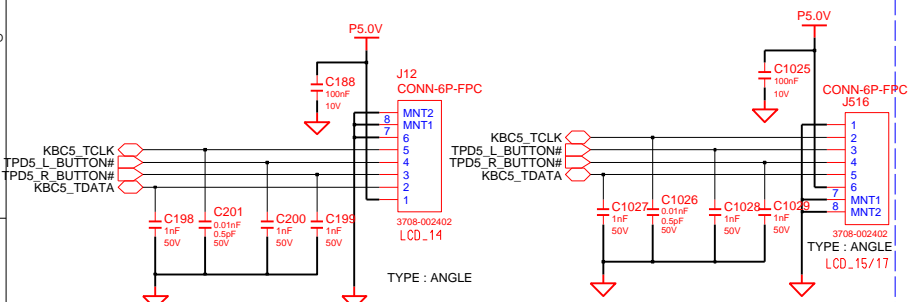
**15.6" & 17.3"****MAIN TO SUB : SATA ODD CONN****SUB TO MAIN : SATA ODD CONN****14"****SATA ODD CONN**LCD\_14  
LCD\_14  
LCD\_14LCD\_15/17  
LCD\_15/17  
LCD\_15/17LCD\_15/17  
LCD\_15/17  
LCD\_15/17MT505  
RMNT-25-65-1P

G\_ODD

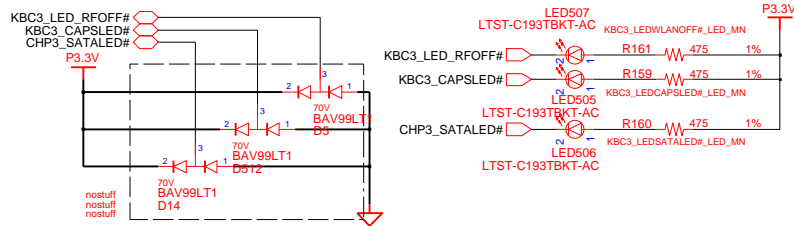
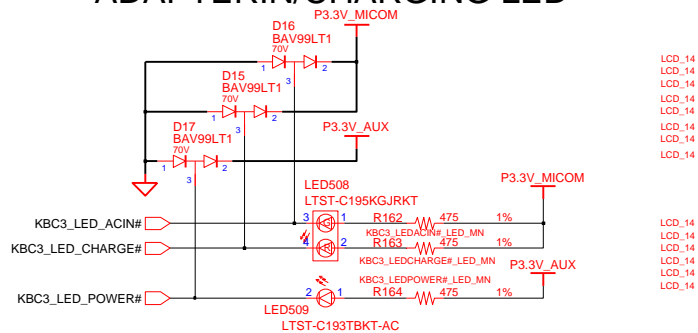
ODD sub board mount hole

DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR	SATA ODD	SATA ODD	
APPROVAL	BL LEE	REV	rev. 1.0	SATA ODD		
MODULE CODE		LAST EDIT		November 22, 2010 15:53:34 PM	PAGE 49 OF 52	PART NO. BA41-01432A

## TOUCHPAD

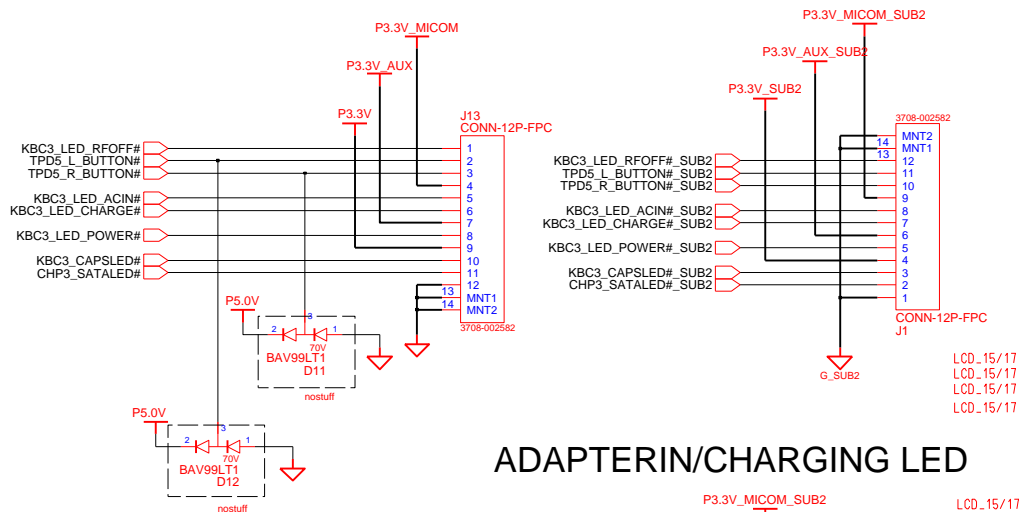


## ADAPTERIN/CHARGING LED

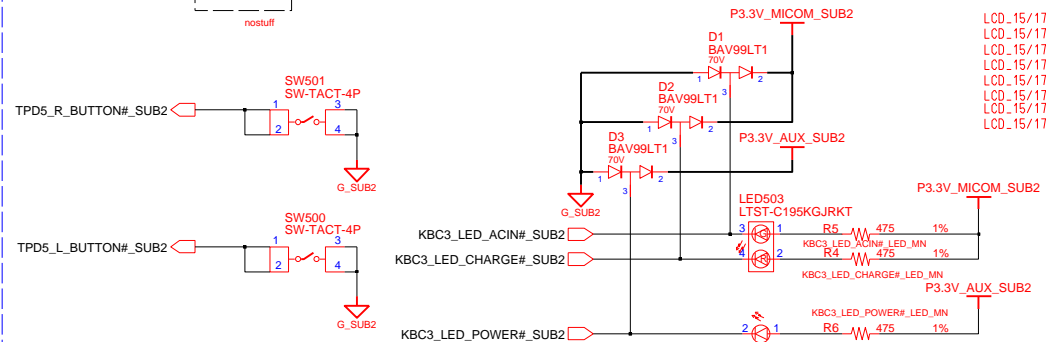


## 15.6" & 17.3"

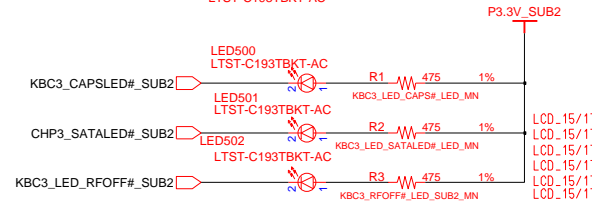
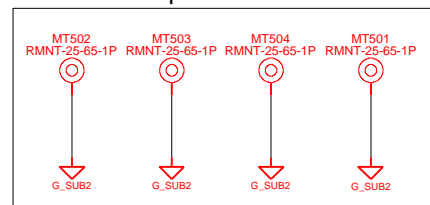
## TOUCHPAD MAIN TO SUB TOUCHPAD SUB TO MAIN



## ADAPTERIN/CHARGING LED

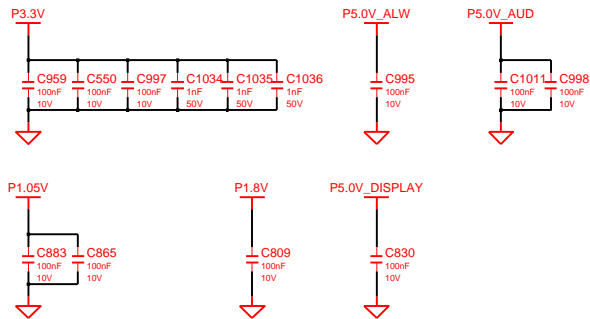



## Touchpad Mount Hole



DRAW	MS YANG	DATE	8/19/2010	TITLE	Jinmao-L Touchpad Touchpad	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01432A
CHECK	MK KIM	DEV. STEP	PR			
APPROVAL	BL LEE	REV	rev. 1.0			
MODULE CODE		LAST EDIT				
November 22, 2010 15:53:34 PM						PAGE 50 OF 52

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DESIGN	MS YANG	DATE	8/19/2010	Jinmao-L MNT hole MNT hole	
CHECK	MK KIM	DEV. STEP	PR		
APPROVAL	BL LEE	REV	rev. 1.0		
MODULE CODE		LAST EDIT		November 22, 2010 15:53:34 PM	PART NO. BA41-01432A
				PAGE	51 OF 52

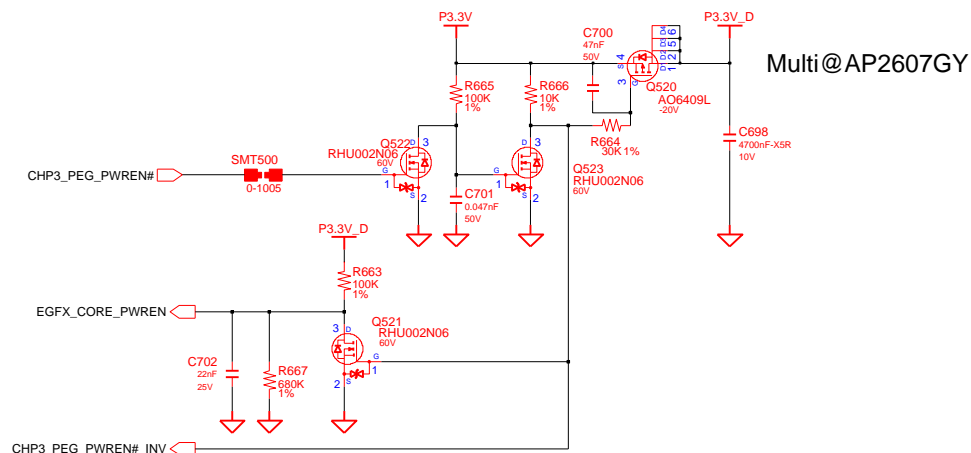
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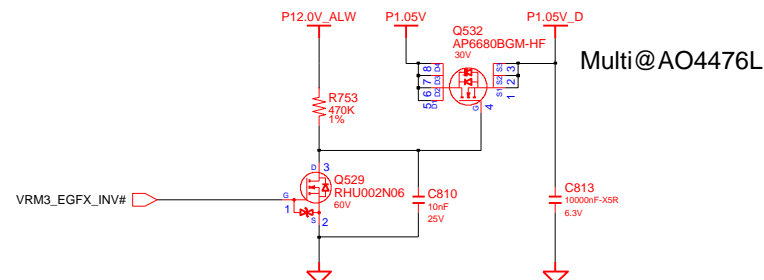
## Switched Power 2 (For nVidia GFX Power Sequence)

Sequence (D3.3V -> GFX Core -> D1.8V -> D1.5V -> D1.05V)

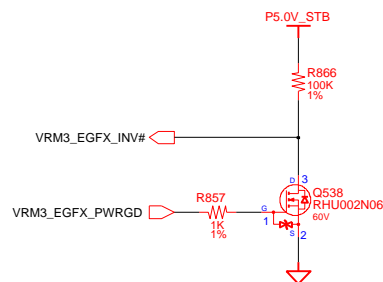
Discrete Switched Power (D3.3V : Max\_1.2A)



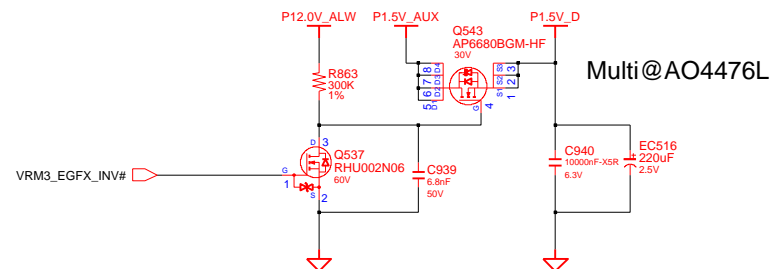
Discrete Switched Power (D1.05V : Max 3.6A)



Discrete Switched Power (D1.8V : Max 0.5A)



Discrete Switched Power (D1.5V : Max 5.0A)



OPT OPT OPT OPT  
OPT OPT OPT OPT  
OPT OPT OPT OPT  
OPT OPT OPT OPT  
OPT OPT OPT OPT  
OPT OPT OPT OPT  
OPT OPT OPT OPT

DRAW	MS YANG	DATE	5/10/2010	TITLE	Jinmao-L	SAMSUNG ELECTRONICS
CHECK	MK KIM	DEV. STEP	PR	Switched PWR 2		
APPROVAL	BL LEE	REV	rev. 1.0	FOR OPTIMUS PWR	PART NO.	BA41-01432A
MODULE CODE		LAST EDIT		November 22, 2010 15:53:34 PM	PAGE	52 OF 52